IMPLEMENTATION OF RIPPLE CARRY ADDER USING ADVANCED MULTILAYER THREE INPUT XOR GATE (TIEO) TECHNIQUE IN QCA TECHNOLOGY

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ABSTRACT

In the present era, transistor reached their highest density and cannot go much smaller than their present size. There are many designs of QCA adders are present in literature, this is new multilayered schematic layout of adder based on QCA technology. In QCA main emphasis on the area and delay reduction leads to an efficient adder design. The proposed adder have less hardware complexity, such as number of cell, delay and total area. QCA designer is the software used form layout generation and simulation results are shown using the coherence vector engine in the same software.

Keywords: full adder, quantum dot cellular automata, three inputs XOR (TIEO) Gate.


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1. INTRODUCTION

QCA is the technology uses arrays of quantum dot cellular automata cells. These arrays of quantum-dot devices, and basic concepts were introduced by Tougaw and Lent in 1993[1]. It has a unique feature that logic states are not stored in voltage levels as in conventional electronics, but they are represented by a cell. A cell is a nano-scale device capable of encoding data by two-electron configuration. The cells must be aligned precisely at nanoscales to provide correct functionality, thus, the proper testing of these devices for manufacturing defects and misalignment plays a major role for quality of circuits [2]
For controlled data flow, clocking scheme is present in QCA Technology controlled by tunneling barrier. In clocking every quantum cell have to go through four stages: locking locked, relaxing and relaxed. QCA have several advantages over a CMOS technology. Some of the advantages include faster switching speeds, high density circuits and low power consumption. Full adder has function of addition and also it is utilized as a core part in other arithmetic operations like subtraction, division and multiplication. So by making adder efficient ultimately reflects to the next generation processing units and electronic machines to be powerful.

This paper is organized as follows. In section 2, we have provided with information about basic concept of QCA technology and next stage one-bit QCA full adder. In section 3, we have proposed our full adder and have demonstrated simulation results. Collected information which is according to previous section, we have compared and analyzed in section 4. Finally, we have concluded the paper in section 5.

2. PRELIMINARY

2.1. Basics of QCA

A quantum dot cellular automaton (QCA) is a promising alternative of the CMOS VLSI technology at a nano-scale designing. A QCA is a cell has four quantum dots with two free electrons for tunneling action. The quantum dot cellular automaton is a novel computing paradigm in nanotechnology that can implement digital circuits with faster speed, smaller size and low power consumption. Quantum cell have one of two states logic 0 or logic 1. Logic state 0 is the polarized P=-1 and logic state 1 is the polarized P=+1 shown in figure 1.

![Quantum Cell](image1)

**Figure 1 Quantum Cell**

The basic building block of QCA Technology is majority voter gate. One majority gate has three inputs and one output. Majority logic is a way of implementing digital operations based on the principles of majority decision. Output will be logical 1 from majority when majority at input is logic 1 and vice-versa. Design Implementation of any circuit is realized by using majority gate and inverter shown in figure 2 and 3.

![3 input Majority Gate and 5 input majority gate](image2)

**Figure 2 3 input Majority Gate and 5 input majority gate**
2.2. Clocking in QCA

For controllable data flow, we have a different clock zones for quantum cells. There are four clock signals in QCA each is phase shifted to 90degree (1/4th the clock signal time) which is shown in figure 4.

For each clock zone we have four clock phases. These clock phases correspond to locking, locked, and relaxing and relaxed shown in figure 5. When cells is at clock phase 0,that is locking state, quantum cell have low potential barriers but are raised during this phase i.e. it takes logic 0 or logic 1 from the input cell or neighbor cell. In the next phase (phase 1) next cell goes in locked state (). At the same time, previous phase cells goes to locked state which is high level period and hold its polarity. In relaxing state, the QCA cell releases its polarity and it’s not affected by the input signals or neighbor cells. Next clock phase is relaxed state the QCA cell goes to the relaxed state. In the relaxed state the QCA cell has no polarity and can’t be affected by neighbor cells.

3. PROPOSED QCA FULL ADDER

Here we present our proposed one bit full adder. The structure of Logical block diagram has been presented in Figure 6. The implementation of full adder is constructed by two gates in three layers. In the main layer carry bit is formed by conventional three input majority gate. In the upper layer we have used three-input XOR (TIEO) gate which is shown in Figure 5(b).

Figure 3 Inverter

Figure 4 Clock Zone scheme in QCA

Figure 5 (a) Logical diagram of full adder [et al, 3]
Proposed QCA one bit full adder has 34 quantum cells and latency of 2 clock phase. There are two engines namely Coherence vector and bistable approximation engines of QCA Designer tool version 2.0.3 are used to verify circuit functional behavior. The fig.6 (a) and fig.6 (b) shows the design of full adder and extracted view of all the three layers. The designer tool illustrates that simulation waveform in Figure 7 has shown correctly result.
3.1. 4-bit Multilayer ripples carry QCA Adder

We use these Full adders as to design N-bit ripple carry adders. For example, Figs. 8, 10, 11 depict the QCA layout of these adders for 4-bit, and 8-bit, 16-bit where the corresponding performance figures will be reported in the next section.

![Figure 8](image1.png) 4–bit Multilayer ripple carry QCA Adder

![Figure 9](image2.png) Output of 4–bit Multilayer ripple carry QCA Adder

![Figure 10](image3.png) 8–bit Multilayer ripple carry QCA Adder

4. COMPARISON AND ANALYSIS

The performance of proposed full adder has been compared with other existing adders in three metrics as shown in Table 1
Table 1

| Adder  | Bit | Cell count | Area(µm²) | Latency
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
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<tbody>
<tr>
<td>Proposed</td>
<td>1</td>
<td>59</td>
<td>0.02</td>
<td>2</td>
</tr>
<tr>
<td>Proposed</td>
<td>4</td>
<td>129</td>
<td>0.11</td>
<td>5</td>
</tr>
<tr>
<td>Proposed</td>
<td>8</td>
<td>257</td>
<td>0.21</td>
<td>9</td>
</tr>
<tr>
<td>Proposed</td>
<td>16</td>
<td>513</td>
<td>0.42</td>
<td>17</td>
</tr>
<tr>
<td>[4]</td>
<td>1</td>
<td>81</td>
<td>1.6</td>
<td>3</td>
</tr>
<tr>
<td>[4]</td>
<td>4</td>
<td>351</td>
<td>1.423</td>
<td>6</td>
</tr>
<tr>
<td>[4]</td>
<td>8</td>
<td>736</td>
<td>1.301</td>
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<tr>
<td>[4]</td>
<td>16</td>
<td>1677</td>
<td>1.452</td>
<td>18</td>
</tr>
</tbody>
</table>

It is usually noted that, multilayer designs are consume much smaller area than their coplanar ones. In our proposed design, the multilayer crossover is used to get high performance. Actually, multilayer crossover is not used for crossing wire; it is just used for construction full adder as intact. Speed of QCA circuit is measured using latency and also it is considered the important metric of the circuit. The proposed adder performs fairly well. Its clocking phase is realized fast. As is shown, our proposed design uses 31 cells, two clock phase and approximately 0.015 µm² area. It can be clearly seen that proposed adder performs fairly well as compared to existing adders.

![Figure 11 16–bit Multilayer ripple carry QCA adder](image)

5. CONCLUSIONS
In this paper, less hardware complexity QCA full adder is presented. It has achieved significant improvements in the terms of cell numbers, area and latency. In addition construction method is also simple to extend to large bit adders. Because the structure consists of two gates, namely three-input majority gate and three input XOR Gate (TIEO)[5]. In the comparison, our proposed full adder has better performance.

We used this technique to design robust and efficient QCA full adders, whose cell count and area consumption are superior to all previous designs. Our adder has cell count is 27% less than [4] for 1-bit QCA design and the 33.33% less latency to [4]. In realization of 4-bit, 8-bit, and 16-bit ripple carry QCA adders, where 63-70% improvement in cell count and 60-80% in area consumption have been achieved, with regard to the best previous ripple carry QCA Adder.

REFERENCES

Implementation of Ripple Carry Adder Using Advanced Multilayer Three Input XOR Gate (TIEO) Technique in QCA Technology


