A 555/690 MSPS 4-BIT CMOS FLASH ADC USING TIQ COMPARATOR

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ABSTRACT

The real world signals are all analog in nature. So in order to convert the analog signals to digital efficiently an “Analog to digital converter” is required. In the digital domain, low power and low voltage requirements are becoming more important issues as the channel length of MOSFET shrinks below 0.25 sub-micron values. These trends present new challenges in ADC circuit design. In this paper, a novel flash analog-to-digital converter for low-power & high speed applications has been proposed by incorporating the threshold inverter quantization technique. The key idea of this technique is to generate $2^n - 1$ different sized threshold inverter quantization comparators for an n-bit converter due to which the fast data conversion speed improves the operating speed and the elimination of ladder resistors leads significant reduction in the power consumption. The use of two cascaded inverters as a voltage comparator is the reason for the technique's name (TIQ). The gain boosters make sharper thresholds for comparator outputs and provide a full digital output voltage swing. The comparator outputs - the thermometer code - are converted to a binary code in two steps through the '01' generator and the encoder. The proposed 4 bit flash ADC using TIQ is designed using FAT tree encoder and simulated with the help of TANNER-EDA tool in 0.25 µm CMOS technology.

This paper represents 4-bit flash ADC for supply voltage of 2.5V and 3.3 V. Also transistor sizes are varied from 1.5µm to 12.1µm for different widths, for input frequency of 1 MHz and speed and power for different variation are estimated. The optimum values of Power and Speed are being chosen amongst the obtained value.

Keywords: Flash ADC, TIQ Comparator, Fat tree encoder.
1. INTRODUCTION

Analog-to-Digital converters are essential building blocks in modern electronic systems. Latest VLSI design trend for signal processing system demands high speed operation and less power consumption. A flash ADC architecture is the faster among known ADC architectures, but limited to lower resolution due to large number of components and high power dissipation. It requires $2^n - 1$ comparators for an n-bit A/D converter.[1]

The speed of an A/D converter is also affected by the type of solid-state technology used to implement the converter. Three different types of solid-state technologies are available for high-speed A/D converter implementation: the CMOS technology, the bipolar technology, and the Gallium Arsenide (GaAs) technology. For this reason, the authors propose an ultrafast CMOS flash A/D converter design featuring the Threshold Inverter Quantization (TIQ) technique. The TIQ technique allows faster A/D conversion speed using the standard CMOS logic circuitry preferred for SOC implementation [2].

The next challenge is low power consumption. ADCs should be integrated with digital circuits on a single chip for the portable devices. All battery powered devices are now being designed to include low power techniques to prolong the battery life. Similarly, ADCs need low power architecture or a low power technique. Low voltage operation is one of the difficult challenges in the mixed-signal ICs[3].

2. THEORY OF ADC

The different types of ADC’s studied in the literature are, 1) Flash ADC, 2) Sigma delta ADC, 3) Ramp counter ADC and 4) Successive approximation ADC. Since flash ADC is the fastest due to its parallel architecture, flash ADC architecture has been widely studied.

A variety of ADCs with different architectures, resolutions, sampling rates, power consumptions, and operating temperature ranges are available. Because of the parallel architecture of flash ADC, all conversions are done in one cycle with many comparators. Flash analog to digital converters, are thus fastest for analog signal to a digital signal conversion. However power consumption and large chip area required for the implementation of flash converters have practical limits at higher resolution although power saving design method for CMOS flash ADC is also available. A Flash ADC using a CMOS inverter based comparator as proposed in under Threshold Inverter technique for high operating speed and low power dissipation using standard CMOS technology [4].

3. RELATED WORK

This section tells about the related work done in designing low power TIQ based flash ADC. Design and implementation of an ultrafast 3-bit 0.25µm CMOS Flash ADC based on TIQ comparator is presented. The TIQ Comparators based ADC is suitable for SoC applications and it is highly adaptable to future semiconductor technologies below 100 nanometer.

This paper [2] presents an ultrafast CMOS flash A/D converter design and performance. Although the featured A/D converter is designed in CMOS, the performance is compatible to that of GaAs technology currently available. To achieve high-speed in CMOS, the featured A/D converter utilizes the Threshold Inverter Quantization (TIQ) technique. A 6-bit TIQ based flash A/D converter was designed with the 0.25 _m standard CMOS technology parameter. It operates with sampling rates up to 1 GSPS, dissipates 66.87mW of power at 2.5 V, and occupies 0.013 mm²area. The proposed A/D
A new power saving design method for CMOS flash ADC is presented in this paper[6]. With an inverter as a comparator along with an NMOS and a PMOS as switches, we use bisection method to let only half of comparators in flash ADC working in every clock cycle. An example of 6-bit flash ADC operates at 200MHz sampling rate and 3.3V supply voltage is demonstrated. The power consumption of proposed circuit is only 40.75mW with HSPICE simulation. Compared with the traditional flash ADC, our bisection method can reduce up to 43.18% in power consumption.

This paper [7] presents the design of an 8-bit FLASH Analog to Digital (A/D) Converter with Threshold Invert Quantization (TIQ) Comparators. Speed of this ADC is 787.78Mbps and the power consumed is 800mW. All individual blocks in this paper are designed and simulated by using T-spice with 0.18 um CMOS Technology.

This paper [8] proposes 4-bit, 1.8V Flash Analog to Digital Converter (ADC) design using CMOS-LTE (CMOS Linear Tunable Transconductance Element) Comparator with 500nm technology. Reference voltages are generated by systematically sizing the transistors of the comparators, thus completely eliminating the resistive ladder network required for the architecture. The total power dissipation observed is 0.28753 mW.

In the paper[9], a 4-bit flash analog to digital converter for low power SoC application is presented. CMOS inverter has been used as a comparator and by adjusting the ratio of channel width and length, the switching threshold of the CMOS inverter is varied to detect the input analog signal. The simulation results show that this proposed 4-bit flash ADC consumes about 12.4 mW at 200M sample/s with 3.3V supply voltage in TSMC 0.35 um process. Compared with the traditional flash ADC, this proposed method can reduce about 78% in power consumption.

4. TIQ COMPARATOR
Threshold inverter quantization (TIQ) is a unique way to generate a comparator for a high speed CMOS flash ADC. A TIQ comparator essentially exploits the voltage transfer characteristic (VTC) curve of an inverter as described in Fig 2. By varying its transistor sizes, the comparison voltage $V_m$ can be changed. Fig 1 shows the comparison of the TIQ comparator and a differential voltage comparator as shown in fig 1 in a traditional flash ADC. Here, the circuits are different but the VTC curves are similar.

The TIQ consists of two cascaded CMOS inverters as shown in Fig. 2. The analog input signal quantization level is set in the first stage by changing the voltage transfer curve (VTC) by means of...
transistor sizing Since the transistor channel length, \( L \), is more effective than the channel width, \( W \), in controlling the performance (\( f_T \alpha 1/L^2 \)), \( L \) is kept constant and only \( W \) is changed during the design process. The second inverter stage is used for increased gain and logic level inversion so that the circuit behaves as an internally set comparator circuit. The key point with the second stage is that the second stage must be exactly the same as the first stage to maintain the same DC threshold levels, and to keep the linearity in balance for the voltage rising and falling intervals of high frequency input signals [9].

A key difference between differential comparator and the TIQ comparator is how to supply their reference voltages. The differential comparator utilizes the external reference voltage \( V_r \) using a resistor ladder circuit. The \( V_r \) directly depends on a resistor tap position. However, the TIQ comparator sets its switching threshold voltage \( V_m \) internally as the built-in reference voltage, based on its transistor sizes. Unlike the conventional flash ADC whose comparators are all identical in size, the TIQ based ADC has individual comparators in all different sizes. To construct an \( n \)-bit flash TIQ based ADC, one must find \( 2^n - 1 \) different inverters, each has different \( V_m \) value. And one must arrange them in the order of their \( V_m \) value [10].

Implemented flash ADC features the Threshold Inverter Quantization (TIQ) technique for high speed and low power using standard CMOS technology. Fig 3 shows the block diagram of the TIQ flash ADC. The use of cascading inverters as a voltage comparator is the reason for the technique’s name.

![Fig 3 TIQ Comparator structure [11]](image)

5. DESIGN OF ADC USING TIQ TECHNIQUE

The block diagram flash ADC using TIQ technique is shown in Fig 4.

![Fig 4 Block diagram of ADC [7]](image)
Design of TIQ Comparator Section

The paper [10], presents design methods and the automation of the comparator circuit layout generation for a flash A/D converter. The threshold inverter quantization (TIQ) based A/D converters require \(2^n-1\) comparators, each one different from all others. Optimal design method of the TIQ comparator presented in the paper [10] significantly improves the linearity of the A/D converter against the CMOS process variation.

The TIQ comparator circuit consists of four cascaded inverters, as shown in Fig. 2. There are four inverters in cascade in order to provide a sharper switching for the comparator and also provide a full voltage swing. The sizes of the PMOS and NMOS transistors in a comparator are the same, but they are different for different comparators. They depend upon the switching voltage they are designed for. The mathematical expression used for deciding these switching voltages is given as

\[
V_{\text{switching}} = \frac{\mu_p W_p}{\mu_n W_n} V_{DD} + V_{tn} + \frac{\mu_p W_p}{\mu_n W_n} V_{tp} + V_{n} \quad \text{(1)} \quad [11]
\]

where, \(W_p\) = PMOS width, \(W_n\) = NMOS width, \(V_{DD}\) = supply voltage, \(V_{in}\) = NMOS threshold voltage, \(V_{tp}\) = PMOS threshold voltage, \(\mu_n\) = electron mobility, \(\mu_p\) = hole mobility, assuming that PMOS length = NMOS length[11].

By varying its transistor sizes, the comparison voltage, \(V_m\), can be changed. However, the TIQ comparator sets its switching threshold voltage, \(V_m\), internally as the built-in reference voltage, based on its transistor sizes. Unlike the conventional flash ADC whose comparators are all identical in size, the TIQ based ADC has individual comparators in all different sizes. To construct an \(n\)-bit flash TIQ based ADC, one must find \(2^n-1\) different inverters, each has different \(V_m\) value, and one must arrange them in the order of their \(V_m\) value. For a 6-bit ADC, 63 individual TIQ comparators are needed [12].

We need \(2^4-1=15\) comparators. As the input analog voltage increases, the comparators start turning on in succession. Thus, we get a thermometer code at the output of the comparators. The point where the code changes from one to zero is the point where the input signal becomes smaller than the respective comparator reference voltage levels. This is known as thermometer code encoding.

Result of a TIQ Comparator

For \(n\)-bit Flash ADC we require \(2^n-1\) TIQ comparators, so we require 15 comparators for 4-bit flash ADC design. This is achieved by varying the widths of PMOS and we get different switching voltages. The output result of the 4-bit TIQ comparator section is shown in the figure 5.
Design of 1 out of n code generator

The output of the comparators in a flash ADC is a thermometer code. This thermometer code is converted to a binary code using an encoder in two steps. The thermometer code is first converted into a 1-out-of-n code using 1-out-of n code generators, which generates a ‘01’ code. This ‘01’ code is converted into a binary code using a fat tree encoder [13].

Fat tree encoder

The thermometer code-to-binary code encoder has become the bottleneck of the ultra-high speed flash ADCs. In this paper, the authors presented the fat tree thermometer code-to-binary code encoder that is highly suitable for the ultrahigh speed flash ADCs.

The fat tree encoder outperforms the commonly used ROM encoder in terms of speed and power for the CMOS flash ADC. The speed is improved by almost a factor of 2 when using the fat tree encoder, which in fact demonstrates the fat tree encoder is an effective solution for the bottleneck problem in ultra-high speed ADCs [13].
The TC (thermometer code)-to-BC (binary code) encoding is carried out in two stages in the fat tree encoder: the first stage converts the thermometer code to one-out-of-N code [13]. This is shown in figure 6. The one-out-of-N code is same as an address decoder output. This code conversion is done in N bit parallel using the gates. The second stage converts the one-out-of-N code to binary code using the multiple trees of OR gates as shown in fig 7.

Fig 7 Fat tree encoder for 4-bit [13]

**Design steps**

1. Design a minimum size inverter and verify the threshold voltage value of the midpoint quantizer, Qn, using the HSPICE circuit simulator by substituting BSIM3 (Level 49) spice model test parameters obtained from a vendor for a specific technology. Note that the channel length is kept at the minimum value during the entire design process.

2. Estimate a safe analog input voltage range as follows: \( \text{Analog range} = Vdd - (VTN + |VTP|) \), where \( VTN \) and \( VTP \) are the threshold voltages for large NMOS and PMOS devices, namely the \( VTHO \) value from the model parameter data set used during the entire design process.

3. Calculate the LSB value as follows: \( \text{LSB} = \text{Analog range} / 2^n \).

Fig 8 Block Diagram of design process [9]

4. Calculate the ideal threshold points for each quantizer (Qn-m … Qn+p) accordingly, assuming the midpoint value for Qn is in the center.

5. Run the HSPICE simulator to obtain the corresponding closest possible channel widths. Note that for the quantizers of Qn+1 … Qn+p), the so-called PMOS side, \((W/L)n \) is kept at minimum value, but only the channel widths of the PMOS transistors are changed to minimize the current flow during the transition of VTC (metastable region). This process is applied to the NMOS side in the opposite way [9].
6. SIMULATION AND RESULTS

In the designing of 4-bit flash ADC, TANNER-EDA tools are used to simulate the schematic circuit and obtain the result. After schematic circuit is simulated using T-Spice tool of TANNER-EDA tool, the result of 4-Bit flash ADC is obtained and is shown in Fig. 9.

![Fig 9 Output of 4-bit flash ADC](a) VDD=2.5V (b) VDD=3.3V

7. CONCLUSION

A simple and fast flash ADC architecture that uses two cascaded CMOS inverters as a comparator, called threshold inverter quantization (TIQ) technique has been proposed and fastest encoder called fat tree encoder has been used. The results are summarized in the following table.

<table>
<thead>
<tr>
<th>Resolution (No. Of Output bits)</th>
<th>4-Bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS Technology</td>
<td>0.250 µm</td>
</tr>
<tr>
<td>Transistor count</td>
<td>436</td>
</tr>
<tr>
<td>Power Supply(VDD)</td>
<td>2.5V</td>
</tr>
<tr>
<td>Max Speed</td>
<td>555 MSPS</td>
</tr>
<tr>
<td>Average Power Consumed</td>
<td>4.0890 mW</td>
</tr>
<tr>
<td>Vm Range(Input Dynamic Range)</td>
<td>0.95V-1.15V</td>
</tr>
<tr>
<td>Vm Distance(VFSR)</td>
<td>0.01333 V</td>
</tr>
<tr>
<td>VLSB</td>
<td>0.00095 V</td>
</tr>
<tr>
<td>Input signal frequency</td>
<td>1MHz</td>
</tr>
</tbody>
</table>
The design is simulated using TANNER-EDA tool. The design and simulation results of 4-bit Flash ADC using 250nm technology have been presented using TANNER-EDA tools. The power supply voltage given is 2.5 V and 3.3 V. However, the circuit should be portable to smaller feature size CMOS technologies with lower supply voltages. Moreover, it is worth noting that the proposed ADC is a clock less circuitry, which is also a reason for the reduced power consumption. However, we further plan to integrate the comparator using latest CMOS technology. Thus, an ADC which is functional at Nano scale CMOS technologies has been successfully designed and demonstrated. The challenges in designing high-speed CMOS flash ADCs are optimizing the speed and power, static and dynamic offset reduction, calibration, and low supply voltage operation.

REFERENCES


