International Journal of Advanced Research in Engineering and Technology (IJARET)
Volume 11, Issue 4, April 2020, pp. 452-460, Article ID: IJARET_11_04_043
Available online athttp://www.iaeme.com/IJARET/issues.asp?JType=IJARET&VType=11&IType=4
ISSN Print: 0976-6480 and ISSN Online: 0976-6499

COMPARATIVE STUDY OF CURRENT STEERING DAC BASED ON IMPLEMENTATION USING VARIOUS TYPES OF SWITCHES

Jayeshkumar J. Patel
Research Scholar, Institute of Technology,
Nirma University, Ahmedabad, India

Dr Amisha Naik
Associate Professor, Institute of Technology,
Nirma University, Ahmedabad, India

ABSTRACT

Digital to Analog Converter (DAC) is a circuit known as a circuit of all seasons. It has wide applications in various fields. Current steering has an advantages over others are in form its speed and power consumption. Non linearity error- Integrated non Linearity (INL) & Differential Non Linearity (DNL) are one of the important measure for DAC and having great impact on the performance of DAC used specifically in the field of medical. Amount of INL and DNL depends on the type of architecture say binary weighted, unary weighted or segmented DAC. Types of switching also have great impact on the INL and DNL. This article presents design and implementation of segmented DAC using various switches like NMOS, PMOS, Transmission Gate and differential switch. The concept of segmented offered the advantage in form of reduction in glitches compared to binary weighted DAC. Looking to Comparison of all, Results of DAC using Differential switch offered an advantage in from of uniform step size on output. Eventually that results in form of better INL and DNL. In order to simulate the design, cadence virtuoso tool with 180 nm MOS technology is used.

Keywords: Analog to Digital Converter. Current-steering DAC, Digital-to-analog converter, DNL, INL, SFDR

Cite this Article: Jayeshkumar J. Patel and Dr Amisha Naik, Comparative Study of Current Steering DAC Based on Implementation Using Various Types of Switches, *International Journal of Advanced Research in Engineering and Technology (IJARET)*, 11(4), 2020, pp. 452-460.
http://www.iaeme.com/IJARET/issues.asp?JType=IJARET&VType=11&IType=4

1. INTRODUCTION

Digital-to-Analog converter (DAC) is a device which takes digital (usually binary) data as input and provides analog signals as output. Analog signal is always continuous in the time domain while the digital signal is discontinuous in the time domain. DACs (Digital to Analog Converters) is known as circuits for all seasons. It has very wide applications in the field of Communication systems, Medicine, Mechatronics, Robotic, etc. DAC may be one of the integrated block of analog-to-digital converters (ADCs) Typically, the DACs are used as output block for microprocessor, microcontroller and/or DSB based system [1],[2]
General structure of N-bit DAC is represented as below in Figure 1

Analog output may be in form of voltage or current and same to be used drive a actuator/s or may be stored. Various types of architectures of DACs are available which includes Current Steering DAC, Weighted R DAC, R-2R Ladder DAC and Charge couple DAC. DAC are evaluated based on Important parameters like, chip area, DFSR, Resolution, offset error, integral non-linearity (INL), differential non-linearity (DNL), gain error, etc [3],[4]

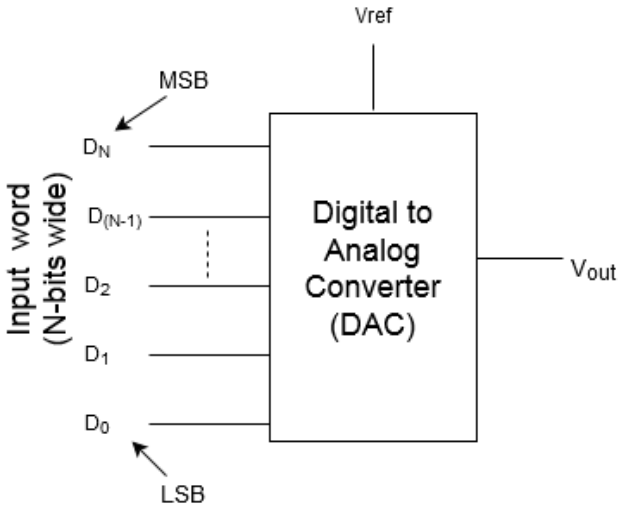

Figure 1 General representation of N-bit DAC

Current steering DACs are widely used because of good switching as output is in form of current. It doesn't need buffer is additional advantage of the same. Non Linearity error (INL and DNL) depends on the switching technology as well as amount of glitches. The concept of differential switch and segmented approach results betterment in form of INL and DNL

2. LITERATURE REVIEW

2.1. Current Steering DAC

Selection of the appropriate DAC depends on the application of the same and for the said application which parameter/s is/are crucial. But in general it is expected to have good performance of DAC in form of linearity error i.e. INL & DNL, gain error, offset error Dynamic performance is affected by non-linearity such as glitches and time skew [6].

Based on the binary inputs, DAC produces a single continuous output value in the shape of current or voltage. The signal which is continuous in amplitude and time domain is obtained from the signal which is discrete in both the said domains with the reference input voltage applied to the data converters. Current steering DAC among various types of DAC's are popular because of the fact that these data converters provide higher resolution with less consumption of power[2],[7].

Digital-to-Analog Converter employing Current Steering topology has higher speed of conversion also supports increased resolution. To improve the matching precision of the current sources the Current Steering DAC is typically employed.

For N-bit DAC, output is expressed as follow:

$$V_{OUT} = \left(D_{N-1}\,2^{N-1} + \mathrm{K} + D_0\,2^0\right)\frac{V_{REF}}{2^N}$$

$$V_{OUT,\max} = \frac{2^{N-1}}{2^N}\cdot V_{REF}$$

Based on the kinds of current sources, Current Steering DACs are mainly classified in two ways namely Binary weighted and Unary weighted Current Steering DAC. In the former case, for N-bit DAC, N number of current sources are required. 4-bit binary weighted DAC is depicted as below shown in Figure 2. It has advantages in form of less no. of current sources and limitations in form of significant glitches due to major transitions of bits.[3][5][10]

In unary DAC, 2^N-1 current sources are required to convert N bit into analog signal. Each current source is having the same current value in this case. 3-bit unary weighted DAC is represented as shown in Figure 3. In this case, advantage is - as there is only one bit change, there will be no glitches. But need more number of current sources which results more area.

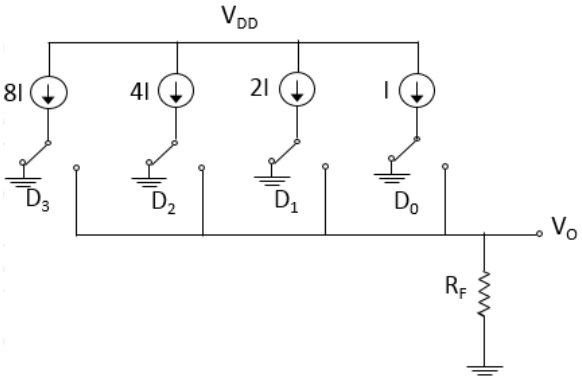

Figure 2 4 bit Current Steering DAC with 4 bit binary weight

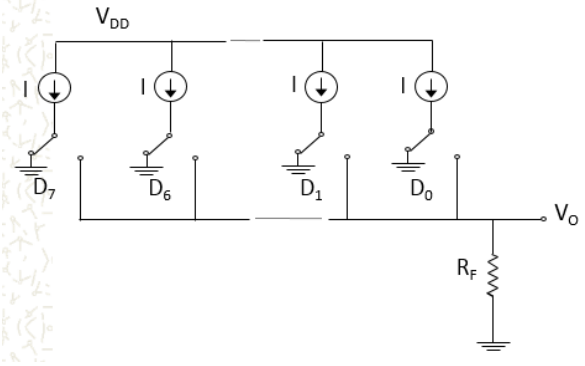

Figure 3 3 bit current Steering DAC with unary weight

A concept of segmented DAC can be used to trade off Static performance of DAC and area as well as power consumption.

The present work is focused to provide following merits over the existing designs reported in last decade. The design objective is to minimize DNL and INL without too much compromising power consumption and chip area for the application in Bio medical field. After carrying out thorough literature survey, simulations and analysis, following modifications are done to bring novelty in proposed DAC.[12]

For the proposed design and simulation, cadence tool is used with 180 nm CMOS technology.

2.2. Segmented Current Steering DAC

INL and DNL mainly depends on glitches in the current cell. Amount and magnitude of glitches depends on no. of transitions of binary inputs. More transitions results more no. of changes the states of switches. In case of 4 bit binary weighted DAC, when input changes from 0111 to 1000, big glitch is observed because of 4 transitions..[3] In case of unary weighted DAC, there is only 1-bit transition so there is no glitch but it needs more no. of current sources; for 4 bit unary current steering DAC, 15 current sources of having same value are required. Thermometer code is used to control the switches. Additional hardware is required to convert

binary code into thermometer codes. Binary to thermometer code conversion for 4 bit is shown in Table 1.

Table 1 Binary to thermometer code representation

Binary code	Thermometer code		Binary code	Thermometer code
0000	000000000000000		1000	000000011111111
0001	000000000000001		1001	000000111111111
0010	000000000000011		1010	000001111111111
0011	000000000000111		1011	000011111111111
0100	000000000001111		1100	000111111111111
0101	000000000011111		1101	001111111111111
0110	000000000111111		1110	011111111111111
0111	000000001111111		1111	111111111111111

To get the benefits of the both say binary weighted and unary weighted DAC, the concept of segmented DAC is explored. For DAC having N inputs, M bits have been implemented using unary weighted DAC while (N-M) bits to be implemented using binary weighted.

Differential nonlinearity (acronym DNL) is a measure of error in DAC. It is defined as the deviation between two analog values corresponding to adjacent input digital values. DNL determines the accuracy of a DAC and can be given as[1][3]:

$$DNL(i) = \frac{V_{out}(i+1) - V_{out}(i)}{ideal\ LSB\ step\ width} - 1$$

Integral nonlinearity (acronym INL) represents a deviation of actual analog output of DAC with reference to expected ideal value for given digital input value. It is also expressed in terms of DNL also. It is as follow.[3]

$$\text{INL (n)} = \sum_{k=0}^{n} DNL(k)$$

2.3. Switching Elements

For current steering DAC, type of switch and its characteristics contribute a lot for the performance of DAC and specifically INL and DNL. Delay time, ON resistance, OFF resistance, ON-Off resistance ratio, parasitic capacitance at output node are some of but very important parameters. Various options are used here like NMOS, PMOS, Transmission Gate and Differential switch. NMOS and PMOS are typical and widely used approach as a switch not only for Digital to Analog convertor but for any digital system. Single signal is required to make it ON or OFF. In case of PMOS, it occupies more area compared to NMOS based switch. For better Resistance characteristics, Transmission Gate is good option. It is parallel combination of NMOS and PMOS devices. Complementary control inputs are required to control Transmission Gate.

2.3.1. Differential Switch

The current-switching structure using NMOS, PMOS or Transmission Gate suffers from dynamic errors. When a switch turns off, the top terminal voltage of its corresponding current source collapses to zero. Thus, the next time that this branch is enabled, the (nonlinear) capacitance at this terminal must charge up, drawing a significant transient current from the output node. Here at the current source a pair of two NMOS transistors are used and controlled by complementary inputs. Hence at a time one stich remains connected to the current source. There will be less effect in from of change in voltage at the output node so dynamic error is less. The ground bounce is much smaller. Of course, one more advantage of this configuration is that it naturally provides differential outputs. [5]

3. SIMULATION RESULTS AND DISCUSSIONS

A 4 bit Binary weighted current steering DAC is implemented in cadence virtuoso 180 nm technology using various types of switches say NMOS, PMOS, Transmission Gate and differential switch. The DAC is simulated with supply voltage of 1.8 V and 200 MHz of the maximum sample rate. By keeping the same voltage and Maximum sampling rate, various approaches are compared based on power consumption, INL and DNL. The concept of segmented is applied to DAC having Differential switch. It has been observed that the glitches have been reduced in case of segmented DAC compared to binary weighted DAC. The design of segmented current steering DAC using differential switch offered a comparative good result among all. It consumes power of 20mW at sampling rate of 200 MHz. For the said DAC, The simulated DNL and INL observed are ±0.36 LSB and ±0.34LSB, respectively.

Architecture of 4 bit binary weighted Current steering DAC using NMOS switches s represented in Figure 4. Transistors Q0, Q1, Q2, Q3 and Q4 are a part of current mirror circuit and are responsible for the current of I, 2I, 4I and 8I. Transistors N1, N2, N3 and N4 are used as a switching elements. Figure 5 shows output in form of current for binary inputs. Major glitches are observed when input changes from 01111 to 10000. One more observation here output is not always increase progressively for all inputs.

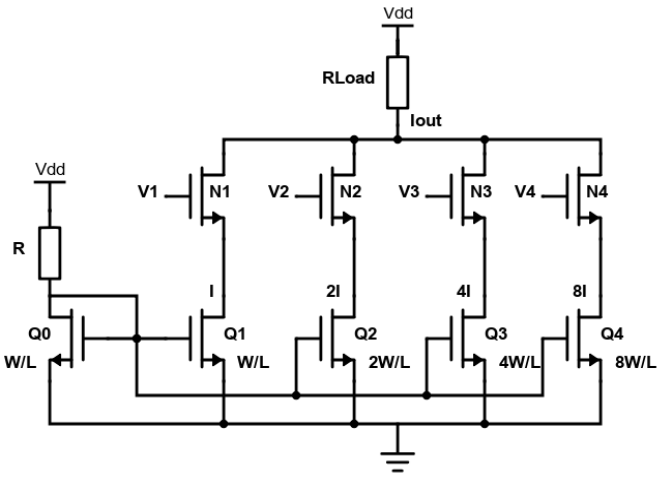

Figure 4 Architecture of 4 bit binary weighted DAC using NMOS switches. [8]

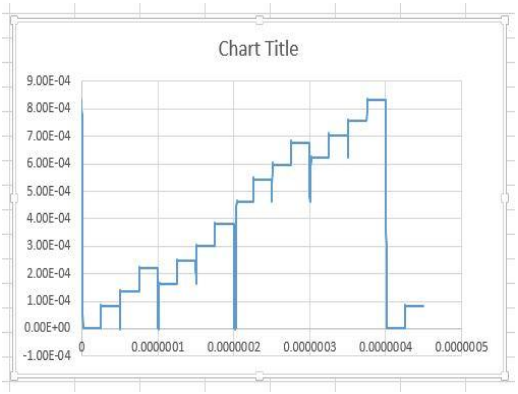

Figure 5 Output :4 bit binary weighted DAC using NMOS switches [8]

By keeping current sources parts same as in case of DAC having NMOS switches, for NMOS transistors (N1. N2, N3 and N4) used as a switches are replaced with PMOS switches MP1, MP2, MP3 and MP4 as shown in Figure 6 . Figure 7 shows an out of the same DAC in form of current. It does not offer any advantages in from of INL and DNL.

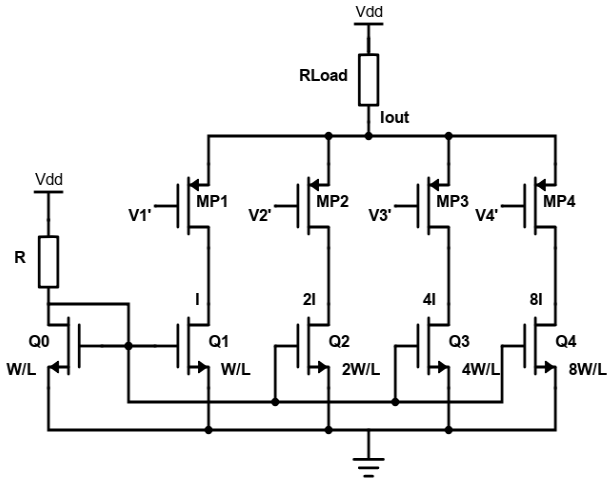

Figure 6 Architecture of 4 bit binary weighted DAC using PMOS switches.

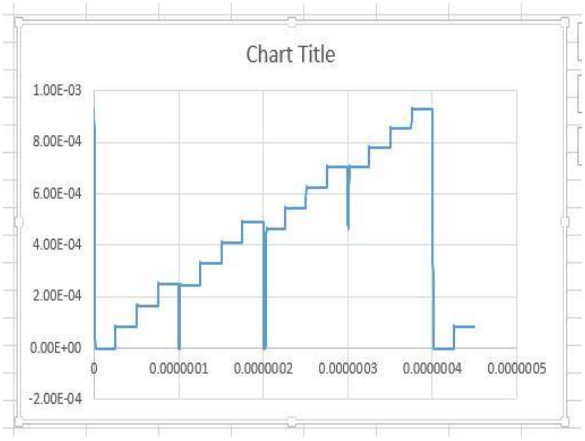

Figure 7 Output of 4 bit binary weighted DAC using PMOS switches

One more architecture is explored having Transmission Gate (TG) as a switching elements having the characteristics of constant resistance. It is made of parallel combination of NMOS and PMOS. It consumes relatively more area compared to options of NMOS and PMOS. The 4 bit current steering DAC using TG switches is shown in Figure 8 and its simulated current output is shown in figure 9 .It has been observed that glitches are there but output increase relatively more uniform compared to previous both cases..

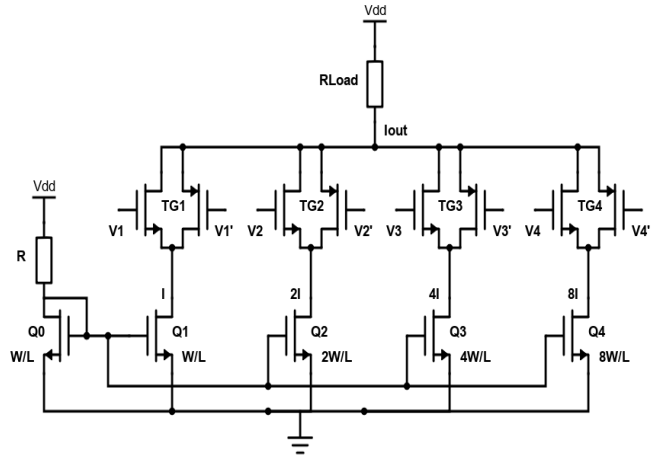

Figure 8 Architecture of 4 bit binary weighted DAC using Transmission gate switches.

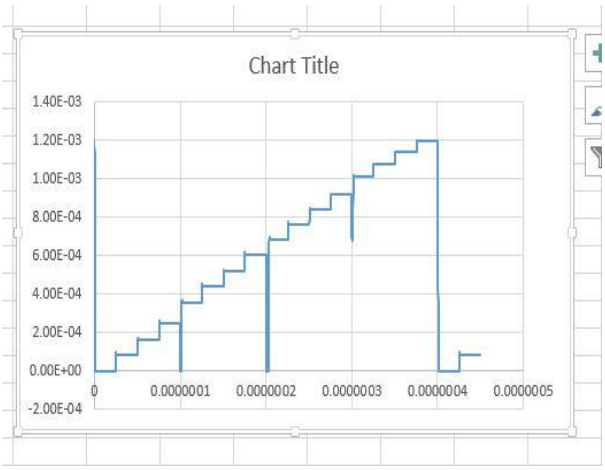

Figure 9 Output of 4 bit binary weighted DAC using Transmission Gate switches

Architecture of 4 bit binary weighted Current steering DAC using Differential switches is represented in Figure 10. Current mirror is same as in previous case. Differential switch (each pair consists of two NMOS transistors) DS1, DS2, DS3 and N4 are used as a switching elements. Figure 11 shows output in form of current for binary inputs. Major glitches are still observed here but more uniform rise in output is observed dislike in case of NMOS, PMOS and Transmission Gate switch cases.

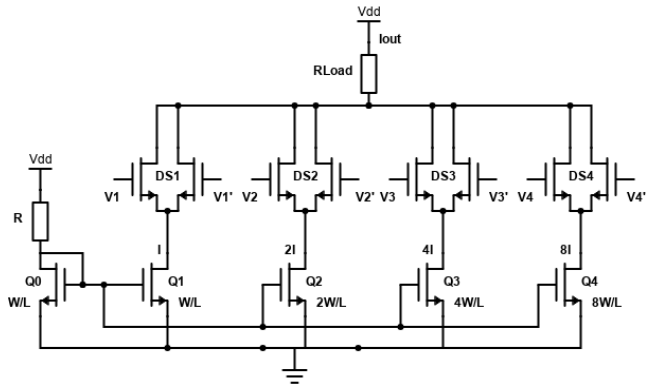

Figure 10 Architecture of 4-bit binary weighted DAC using Differential switches [8]

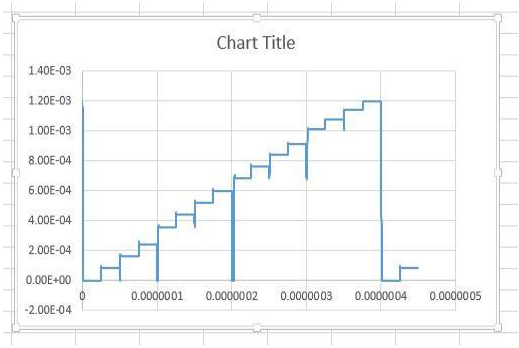

Figure 11 Output of 4-bit binary weighted DAC using Differential switches [8]

To address the problem of glitches, the concept of Segmented DAC is used here. Here Differential switches have been used There are two options are explored (a.) LSBs are implemented using Unary current sources and MSBs are implemented using Binary current sources. Current output of the same is represented in Figure 12. (b) LSBs are implemented using Binary current sources and MSBs are implemented using Unary current sources. Current output of the same is represented in Figure 13

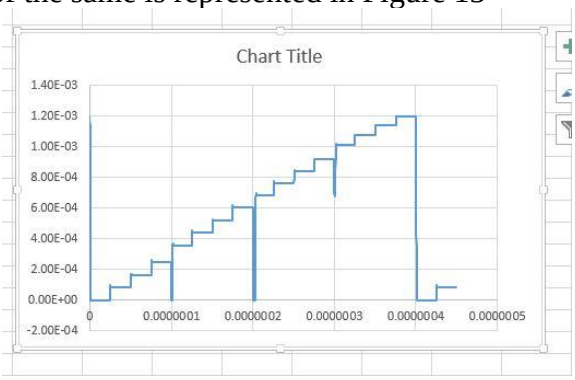

Figure 12 Output of segmented DAC using Differential switches (LSBs are Unary and MSBs are Binary sources)

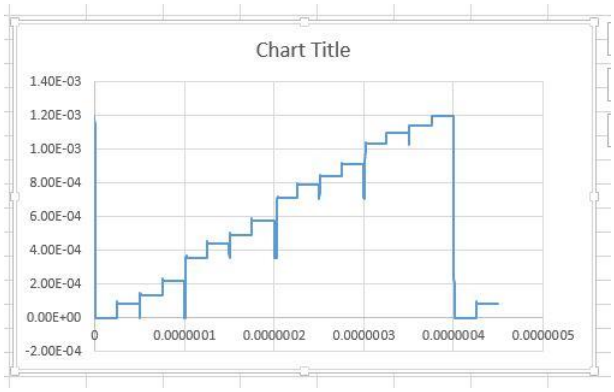

Figure 13 Output of segmented DAC using Differential switches (LSBs are Binary and MSBs are Unary sources)

Here it is observed that Differential switches with Segmented DAC offers advantages in from of reduction in glitches and uniform rise in output which results in reduction of non-linearity error (INL and DNL). Graphs for INL and DNL of proposed segmented Current steering DAC with Differential switches are represented in Figure 14 and Figure 15 respectively.

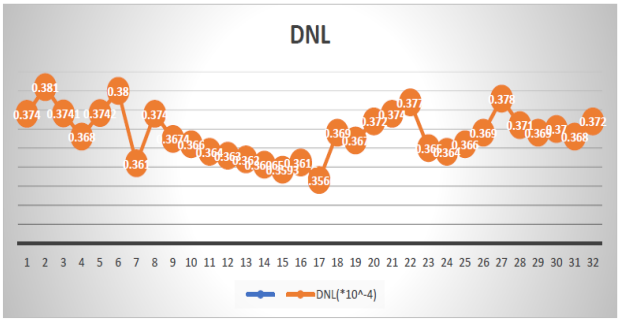

Figure 14 DNL graph of 4 bit segmented DAC with differential switch

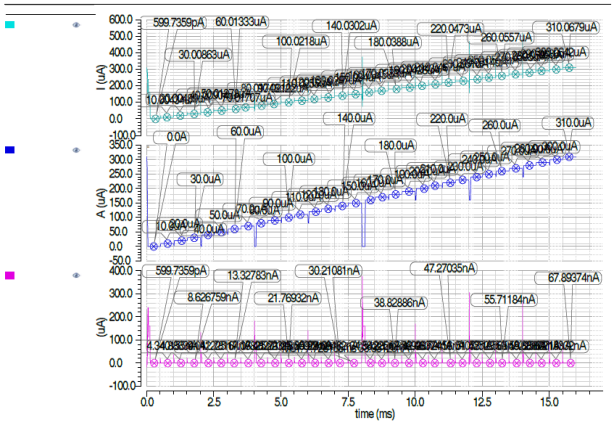

Figure 15 Plot of INL 4 bit segmented DAC with differential switch

Comparison of 4 bit segmented current steering DAC using different switches are as shown in Table 2

Table 2 Parameter comparison of current steering DAC

Parameters	Simulated Value			
	NMOS Switch	**PMOS Switch**	**Transmission Gate switch**	**Differential switch**
Technology	180	180	180	180
Resolution	4 bit	4 bit	4 bit	4 bit
Approach	Binary weighted	Binary weighted	Binary weighted	**Segmented**
Supply voltage	1.8 V	1.8 V	1.8 V	1.8 V
INL (Max)	0.63 LSB	0.7 LSB	0.54 LSB	**0.34 LSB**
DNL (Max)	0.56 LSB	0.72LSB	0.43 LSB	**0.36 LSB**
Power (Max)	14mW	18mW	26mW	20mW
Frequency	200 Mhz	200 Mhz	200 Mhz	200 Mhz

4. CONCLUSION

From Result and Discussions, at the frequency of 200 Mhz with supply voltage of 1.8 V, it has been observed that the Static error (INL and DNL) in the output current of the DAC mostly depends on type of switch, speed of switching. The result of DAC having Differential switch shows reduction in glitches as well as uniformly increase in output with reference to Digital inputs. which results in improvement in INL and DNL values. It is also observed that Segmented DAC having better performance in from of INL and DNL as well as glitches compared to Binary weighted DAC. A Current DAC using differential switch offers a desirable performance in form of DNL and INL which is in the range of $\pm$0.5 LSB.

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