DESIGN AND SIMULATION OF ARITHMETIC LOGIC UNIT USING QUANTUM DOT CELLULAR AUTOMATA

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ABSTRACT

Quantum Dot Cellular Automata (QCA) is a modern paragon that encodes binary information, i.e. 0 and 1, inside a cell instead of traditional current switches. Information is expressed by a QCA cell’s charging configuration. Current does not flow in these cells. This innovative concept provides a potential alternative to transistor-less computation at Nano scale.

An ALU stands for Arithmetic Logic Unit which carries of logical and arithmetic operation based on the input operands.

The concept of layering is used to give input to the proposed Arithmetic Logic Unit (ALU), thus reducing the occupation area and the cell count. It consists of Half Adder and NAND Gate followed by two 2x1 Multiplexer. The proposed design of half adder and NAND Gate (used for And operation) uses less occupation area, less number of cells and low energy dissipation than the existing designs.

Keywords: QCA - Quantum Dot Cellular Automata, nanotechnology, multilayer, ALU – Arithmetic Logic Unit.

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1. INTRODUCTION

1.1. QCA Background

Lent et al proposed Quantum-Dot Cellular Automata to introduce classic cellular automaton with quantum dots. Quantum dots are nanoscale structures, constructed from Semiconductors such as GaAs.
Design and Simulation of Arithmetic Logic Unit Using Quantum Dot Cellular Automata

The QCA circuits comprises of quantum cells which further consist of four quantum dots. In QCA, circuits are fabricated by quantum cells, and each cell contains as well as two electrons. The transfer of information is accomplished through the change in polarization state rather than electron flow in CMOS, which further reduces power dissipation, delay and increases equipment density.

A small number of QCA based Arithmetic and Logic Units have been proposed so far. In this project, we are simulating an Arithmetic Logic unit consisting of Half Adder and Nand gate.

1.1.1. QCA Cells
“A QCA cell is a nano structure with four quantum dots as illustrated in the fig.1. Two electrons can tunnel between four quantum dots.” Binary information is represented using two electrons positioned in each logic cell that are set in opposite dots as shown in the fig. 2(a) and 2(b).

(a) Binary 0 (P = -1)  (b) Binary 1 (P = 1)

Figure 1 Cell with four Quantum Dots  Figure 2 Quantum Cells with Polarization

1.1.2. QCA Basic Gates
“QCA consists of 2 types of simple logic gates, inverter and a three-input majority gate. Three- input majority gate can be used to consists AND and OR gate.”

(a)Inverter  (b) Three Input Majority Gate

Figure 3 Basic Gates

1.1.3. QCA Wire Crossings
The most significant characteristics of QCA is its capability to create various signal wire crossings. There are two crossover options available: Coplanar and Multilayer crossovers.

Coplanar Crossing
This was introduced for QCA architecture that uses a single layer to introduce crossovers, as shown in fig.4. It uses both rotated as well as regular cells. The two groups of cells when correctly aligned with each other tend to not interact with each other. Previous research hints coplanar crossings to be very susceptible to misalignment and adversely effected by noise.

Multilayer Crossing
The other option is the Multilayer crossing, which requires more than one layer of cells, as shown in Fig. 5. It is deduced that Multilayer crossovers comparatively produces robust simulation outputs. However, multilayer crossovers is not easy to manufacture, and the
expense of making of multilayer crossover is estimated to be considerably high as compared to that of coplanar crossover.

1.1.4. QCA Clocking Schemes

The basic requirement for the functioning of a QCA circuits is clock, it’s required to synchronize and control the flow of information through the QCA wires.

By controlling the potential barrier of the cells in a QCA wire we can create the clocking effect. There are 4 clocking zones in QCA namely: relax, release, hold and switch, each of the four clocks have a phase difference of 90° each.

1.2. ALU Background

An ALU stands for Arithmetic Logic Unit which carries logical and arithmetic operation based on the input operands. Arithmetic operations consists of addition, subtraction, multiplication and division. Whereas logical operations consists of AND, OR and NOT. Implementation of ALU in QCA results in the improvement of parameters like area, cell count, and power dissipation as compared to CMOS, a transistor based technology.

1.2.1. Universal Gates

There are 2 types of Universal gates, NAND gate and NOR gate which can be connected to create Inverter, AND Gate and OR Gate.

NAND Gate
Table 1 Truth Table of NAND Gate

<table>
<thead>
<tr>
<th></th>
<th></th>
<th>NAND</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

1.2.2. Combinational Circuits
Half Adder and Half Subtractor

![Figure 8 Realization of Half Adder](image)

![Figure 9 Realization of Half Subtractor](image)

Table 2 Truth Table of Half Adder and Half Subtractor

<table>
<thead>
<tr>
<th></th>
<th></th>
<th>SUM</th>
<th>CARRY</th>
<th>DIFF</th>
<th>BORROW</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

2. QCA IMPLEMENTATION OF ALU
This paper suggests a 2-bit ALU design. The block diagram is shown in fig. 10.

![Figure 10 Block Diagram of Proposed Arithmetic Logic Unit](image)

QCA Designer has been used to create Arithmetic Logic Unit. It is a software tool for designing and simulating QCA Circuits. Here, Blue and Yellow cells are Input and Output cells respectively. The Orange cell is of fixed polarization as shown in 1.
NAND Gate is implemented in QCA as shown below.

![QCA Layout of NAND Gates](image1)

**Figure 11** QCA Layout of NAND Gates

Figures 12 (a) and (b) depicts Half Adder and Half Subtractor

![QCA Layout of Combinational Circuits](image2)

**Figure 12** QCA Layout of Combinational Circuits

![QCA Layout of Arithmetic Unit](image3)

**Figure 13** QCA Layout of Arithmetic Unit

The ALU illustrated in fig.13 has the input through the concept of layering.
3. SIMULATION RESULTS
The results of all the circuits tested are presented in Figures 15, 16, 17 for all the basic logic gates, NAND Gate and combinational circuits respectively.

QCA Designer-E is a tool for estimation of energy dissipation.

Figure 14 QCA Layout of Arithmetic Logic Unit

Figure 15 Resultant Graph of NAND Gate

Figure 16 Resultant Graph of the Arithmetic Unit
4. COMPARITIVE ANALYSIS

This proposed design has 0.61 micrometer square occupation area, 294 cells and multilayer wiring. Cross wiring with four clocks are used for the flow of the information. The design proposed is efficient in terms of cell count required as compared to the existing ALU design. Table 5 shows performance analysis of different ALU designs.

The performance of Proposed and Existing designs of NAND Gate are displayed in Table 3. The comparison table for different Half Adder designs is given in Table 4.

Table 3 Performance Analysis of different designs of NAND Gate

<table>
<thead>
<tr>
<th>NAND Gate Designs</th>
<th>Cell Count</th>
<th>Energy Dissipated(eV)</th>
<th>Area(square nanometers)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[6]</td>
<td>12</td>
<td>0.00379</td>
<td>15960</td>
</tr>
<tr>
<td>[7]</td>
<td>8</td>
<td>0.00362</td>
<td>13098</td>
</tr>
<tr>
<td>Proposed Design</td>
<td>5</td>
<td>0.000596</td>
<td>4234</td>
</tr>
</tbody>
</table>

Table 4 Performance Analysis of different designs of Half Adders

<table>
<thead>
<tr>
<th>Half Adder Designs</th>
<th>Cell Count</th>
<th>Energy Dissipated(eV)</th>
<th>Area(square nanometers)</th>
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</thead>
<tbody>
<tr>
<td>[3]</td>
<td>79</td>
<td>0.023</td>
<td>103878</td>
</tr>
<tr>
<td>[8]</td>
<td>48</td>
<td>0.0158</td>
<td>53410</td>
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<tr>
<td>Proposed Design</td>
<td>21</td>
<td>0.0126</td>
<td>22914</td>
</tr>
</tbody>
</table>

Table 5 Performance Analysis of Without Layering, Existing and Proposed Designs of ALU

<table>
<thead>
<tr>
<th>PARAMETERS</th>
<th>Without Layering</th>
<th>[1]</th>
<th>Proposed Design</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cell Count</td>
<td>327</td>
<td>324</td>
<td>294</td>
</tr>
<tr>
<td>Energy Dissipated(eV)</td>
<td>0.114</td>
<td>0.134</td>
<td>0.098</td>
</tr>
<tr>
<td>Crossover Type</td>
<td>No Crossover</td>
<td>Multilayer</td>
<td>Multilayer</td>
</tr>
<tr>
<td>Energy Dissipated (eV) per cycle</td>
<td>0.0103</td>
<td>0.0121</td>
<td>0.00907</td>
</tr>
<tr>
<td>Simulation Time</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
</tbody>
</table>

Figure 17 Resultant Graph of the proposed Arithmetic Logic Unit
5. CONCLUSION
The proposed design of NAND Gate and Half Adder are much faster and utilizes less area than the existing designs as shown in tables 1 and 2. The proposed design of Arithmetic Logic Unit which is based on multilayer concept is supreme to the Coplanar ALU designs as it utilizes less area than the contrary as shown in table 3, hence satisfying the essence of Nano technology. This circuit shows improvement in the parameters used in the evaluation of QCA circuits.

REFERENCES