OPTIMIZATION OF DIGITAL COMPARATOR USING TRANSMISSION GATE LOGIC STYLE

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ABSTRACT
In the present scenario low power, speed and size play a significant role specifically in the field of digital VLSI circuits. The major goal of this paper is to design and implement of digital comparator the usage of proposed transmission gate logic method and compared in terms of power consumption, propagation delay and transistor count. The results of this paper are simulated on the EDA tanner tool realized in 0.25-micrometer technology.

Key words: Digital comparator, CMOS logic, transmission logic gate, power consumption, delay, transistor count.

http://www.iaeme.com/IJARET/issues.asp?JType=IJARET&VType=7&IType=4

1. INTRODUCTION
The power consumption is a vital issue in digital CMOS circuits, where different techniques and technologies are used to design circuits for low power dissipation with small size and high-speed interface applications are developed.

The smaller size, higher circuit speed, and lower power dissipation have been a central point in today's PCs and correspondence frameworks that offer more
noteworthy execution altogether diminished cost per work, and should decrease the physical size, in the examination with their forerunners.

Circuit size relies on upon the quantity of transistors and their sizes and on the wiring complexity [1]. The wiring intricacy is dictated by the quantity of associations and their lengths. Therefore, the wiring complexity may fluctuate significantly from one logic style to another and consequently, the legitimate decision of logic style is critical for circuit execution [2].

Digital comparator has several utilities like those are utilized as a part of the scene deciphering hardware in PCs and chip based gadgets to prefer a particular input/output device for the capacity of information, in control applications in which the parallel numbers representing to physical variables, such as, temperature, position, and so on are contrasted and a reference esteem. At that point, the output of the comparator is used to drive the actuators to build the physical variables nearest to the set or reference esteem.

In this paper, a modified digital comparator using the CMOS transmission gate logic has been designed with the low power consumption and higher packing densities and compare with other logic techniques in 0.25-micrometer technology.

2. TWO-BIT DIGITAL COMPARATOR

In digital logic system, the traditional method of comparison of two variable A \( (A_0, A_1) \) and B \( (B_0, B_1) \) of a two-bit binary number is a logical operation that figures out whether A is less than B, A is greater than B and A equal to B [3], [4]. Therefore, the digital comparator is such type of logic circuit that thinks about the relative magnitudes of these two variables. The block diagram of digital comparator appears in Figure 1. The result of digital comparator is determined by three variables that demonstrate whether A>B, A<B, or A=B.

![Figure 1. Block Diagram of Digital Comparator.](image)

The first step in the comparison processor of the two-bit digital comparator is to check the greatest bit \( A_0 \) and \( B_0 \). On the off chance that greatest bit of both inputs are distinctive, e.g. assume the greatest bit of A is more prominent than B in that case A>B and if the greatest bit of B is more prominent than A at that moment A<B. In the event, that greatest bit of both inputs is equivalent after that go for next step. The second step is to check the following relating bits \( A_1 \) and \( B_1 \) of both the inputs. On the off chance that next comparing bit of A is more noteworthy than B at that moment A>B and if information condition is switch, subsequently A<B. In the event that, both
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inputs are same subsequently A=B [7]. Equation (1), equation (2) and equation (3) is given to control the outputs of the two-bit digital comparator.

Table I. Truth Table of Two-Bit Digital Comparator

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0</td>
<td>A1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
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<td>0</td>
<td>0</td>
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<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

The output of digital comparator is determined by using truth table.

\[
A > B: = A_0\overline{B}_0 + A_1\overline{B}_1 (A_0 \text{EX} - \text{NOR} B_0) \\
= A_0\overline{B}_0 + A_1\overline{B}_1 (A_0 \text{EX} - \text{NOR} B_0) \\
\text{(1)}
\]

\[
A < B: = \overline{A}_0B_0 + \overline{A}_0A_1\overline{B}_0B_1 + A_0\overline{A}_1B_0B_1 \\
= \overline{A}_0B_0 + \overline{A}_1B_1 (A_0 \text{EX} - \text{NOR} B_0) \\
\text{(2)}
\]

\[
A = B: = \overline{A}_0A_1\overline{B}_0\overline{B}_1 + \overline{A}_0A_1B_0B_1 + A_0A_1B_0B_1 + A_0\overline{A}_1B_0\overline{B}_1 \\
= (A_0 \text{EX} - \text{NOR} B_0) (A_1 \text{EX} - \text{NOR} B_1) \\
\text{(3)}
\]

The gate implementation of a two-bit digital comparator is shown in Figure 2. Equation (1), equation (2) and equation (3) is given for the outcome of two-bit digital comparator.
3. TWO-BIT DIGITAL COMPARATOR DESIGN USING CMOS LOGIC STYLE

In the present situation low power and rapid are imperative factors in the field of digital VLSI circuits. Since CMOS consumes less power and provides high speed, therefore it is considered as the best alternative design process in the digital circuit. In this technique, a circuit consists of two networks, one NMOS pull-down network, which connects the output to the ground and another PMOS pull-up network, which connects the output to supply ($V_{dd}$). The CMOS logic circuit is outlined in a way that stands out system is directing at once. The CMOS logic technique is shown in Figure 3.

In the event that the voltage of a low logic level is applied to the input, subsequently, PMOS is in ON condition and give a low impedance path from $V_{dd}$ to the output. In this way, the output goes to a high level of $V_{dd}$. If the voltage of a high logic level is connected to the input, and at that time NMOS is in ON condition and give a low impedance path from the ground to the output. Hence, the output goes to a low logic level of 0V. The substrate of NMOS is always connected to the ground while the substrate of PMOS always connects to $V_{dd}$. CMOS logic style is really an extension of CMOS inverters to multiple inputs [5]. The two-bit digital comparator using the CMOS logic technique is shown in Figure 4.
4. TWO BIT MAGNITUDE COMPARATOR USING PASS TRANSISTOR LOGIC (PTL) STYLE

Pass transistor logic gives better speed and less power dissipation than conventional CMOS because this design style requires less number of transistor. Main idea behind PTL is to use purely NMOS Pass Transistors network for logic operation [1]. The basic difference of pass-transistor logic style compared to the CMOS logic style is that the source side of the logic transistor networks is connected to some input signals instead of the power lines as in Figure 8. In this design style, transistor acts as switch to pass logic levels from input to output [3].

5. CMOS TRANSMISSION GATE LOGIC

The transmission gate logic gives high speed and less power dissipation than conventional CMOS for the reason that of the small transistor stack height, the least number of transistors is required and no complementary input signals are required. The transmission gate comprises of one NMOS and one PMOS transistor, which are associated in parallel. The graphical symbol of the transmission gate appears in Figure 5.
It will act as a switch which selectively block or pass a signal from the input to the output by biasing the control gates in a complementary way according to the demand. The truth table of the transmission gate logic is shown in Table II.

**Table II. Truth Table of Transmission Gate Logic**

<table>
<thead>
<tr>
<th>Control Input (g)</th>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>High logic level</td>
<td>High logic level</td>
<td>High logic level</td>
</tr>
<tr>
<td>Low logic level</td>
<td>Don’t care (x)</td>
<td>High Impedance</td>
</tr>
</tbody>
</table>

If the voltage on node g is a high logic level (g=1), after that, both transistors are ON and give a low impedance path between input and output, so a signal can easily pass from input to the output. If the voltage on node g is a low logic level (g=0), after that, both transistors are OFF and give the high impedance path between input and output, therefore, no signal can pass from input to the output.

6. TWO-BIT DIGITAL COMPARATOR USING TRANSMISSION GATE LOGIC STYLE

The schematic of the existing transmission gate logic based two-bit magnitude comparator is shown in Figure 7 which consists of 66 transistors [6]. Due to a large number of transistors, it will consume more power and lower packing density. But in nowadays as the power, speed and area are the significant factors in digital VLSI circuit. As a result, this designed is not considered for superior performance. Consequently, this paper concentrated on modified transmission gate based two-bit digital comparator designed which consists of 30 transistors only. In this proposed design the power consumption is reduced with larger packing density and higher speed. In the proposed design each transmission gate act as an AND gate which is used in conventional gate design of the two-bit digital comparator. Subsequently, the circuit required the least number of transistors. The proposed transmission gate based two-bit digital comparator appears in Figure 8.
7. SIMULATION RESULTS
The simulation result is measured by the EDA Tanner tool. We inspected our circuit for various inputs $A_0=110011$, $A_1=001111$; $B_0=111100$, $B_1=001111$. The schematic circuit configuration of CMOS logic, pass transistor logic and proposed transmission gate logic based two-bit digital comparator and its output power waveform are appearing in Figure 9, 10, 11, 12, 13 and 14 respectively. The simulation result is abridged in Table III.
Optimization of Digital Comparator using Transmission Gate Logic Style

Figure 9. Schematic of the Two-Bit Digital Comparator using the CMOS Logic Technique.

Figure 10. Simulation Output Pattern of the Two-Bit Digital Comparator using the CMOS Logic Technique.

Figure 11. Schematic of PTL Based 2-Bit Magnitude Comparator.
Figure 12. Simulation Output Pattern of PTL Based 2-Bit Magnitude Comparator.

Figure 13. Schematic of the Proposed Two-Bit Digital Comparator.

Figure 14. Simulation Output Pattern of the Proposed Two-Bit Digital Comparator.
Table III. Performance Comparison of Two-Bit Digital Comparator

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Conventional</th>
<th>TG logic</th>
<th>Proposed TG logic</th>
<th>PTL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power consumption (µW)</td>
<td>10.55</td>
<td>7.52</td>
<td>4.83</td>
<td>4.81</td>
</tr>
<tr>
<td>Number of transistor</td>
<td>54</td>
<td>66</td>
<td>30</td>
<td>40</td>
</tr>
<tr>
<td>Propagation delay (n-sec)</td>
<td>10.40</td>
<td>10.49</td>
<td>10.34</td>
<td>9.73</td>
</tr>
<tr>
<td>Power delay Product (µ-nJ)</td>
<td>109.72</td>
<td>78.89</td>
<td>49.94</td>
<td>46.80</td>
</tr>
</tbody>
</table>

8. CONCLUSIONS

To improve the performance of 2-bit magnitude comparator we have designed modified transmission gate logic based magnitude comparator. After simulation of all type of design techniques final results are obtained for Power Consumption, Delay and Power Delay Product. Power consumption of both proposed TG and pass transistor logic based 2-bit magnitude comparator has almost same. Power consumption of the proposed 2-bit magnitude comparator is 4.83µW which is almost 35.77% less than existing transmission gate logic based 2-bit magnitude comparator. Pass transistor logic style provide less Power Delay Product as compared to other techniques. It has been found that the transistor count is less in the proposed TG logic circuit as compared to other techniques, so that the overall area is minimized. After simulation it has been found that the Pass transistor logic technique does not provide full output voltage swing which is one of the drawbacks of pass transistor logic.

REFERENCES


