Three-Dimensional Analytical Subthreshold Current Model of Fully Depleted SOI MOSFET's

Krishna Meel¹, Ram Gopal², Deepak Bhatnagar³

¹²MEMS & Micro-sensor Group, CSIR-Central Electronics Engineering Research Institute, Pilani (Rajasthan), India
³Department of Physics, University of Rajasthan, Jaipur (Rajasthan), India

¹krishna.meel@bkbiet.ac.in

ABSTRACT: A new 3-D analytical model of subthreshold current based on the three dimensional analytical solution of Poisson's equation with suitable boundary conditions of enhancement mode fully depleted SOI-MOSFET is presented in this paper. The effect of channel length, width and doping concentration for uniformly doped SOI MOSFET has been investigated. The results obtained from the proposed model have been compared for validation with ATLAS device simulator.

KEYWORDS: SOI MOSFET, Green’s Function, Three-dimensional, Subthreshold current model, ATLAS Software.

I. INTRODUCTION

As the device dimensions are shrinking below sub-micron range a new SOI technology replaces the MOS technology to meet the requirement of today’s high speed and low power circuits. Enhancement mode fully depleted SOI MOSFET have several advantages over CMOS MOSFETs such as better immunity to short channel effects[1], improved subthreshold slope, saturation current enhancement[2],punch-through suppression, high transconductance and so on. The sub-threshold characteristic of SOI MOSFET is a very important parameter to be determined to meet the present requirements of a transistor, therefore, accurate model for the subthreshold current is of a great help for the designers of SOI MOSFETs.

Although the 3-D analytical modeling of threshold voltage of fully depleted SOI MOSFET has been carried out by some of the authors [3,5] but no model related to sub-threshold characteristics is available in the literature to the best of our knowledge. Here we are presenting a new three-dimensional sub-threshold current model of fully depleted uniformly doped SOI MOSFET. The model considers drift as well as diffusion components of sub-threshold current and also DIBL effects are taken into account. The model is based on the analytical solution of 3-D Poisson's equation within the depleted SOI film. It provides a convenient tool to determine the threshold voltage and sub-threshold characteristics of the device.
II. Subthreshold Current Model

Fig. 1 shows the cross sectional view of fully depleted n-channel SOI MOSFET along the channel length, $L$ and width, $W$. The origin $O(0,0,0)$ is assumed to be situated at the center of front gate oxide-silicon interface. The thickness of front gate oxide is $t_{ox}$, back gate oxide is $t_{si}$, side oxide is $t_{box}$ and that of SOI film is $t_{soi}$. The front gate and back gate voltages are defined as $V_{Gf}$ and $V_{Gb}$ respectively. The voltage at drain end is $V_D$ while that of source end is grounded.

In this paper the effect of doping concentration and channel length on subthreshold current, is analysed. The expression of surface potential is taken from our earlier publication [6] which
is used to formulate a new 3-D subthreshold current model. The analytical approximate expression for surface potential, \( \phi(x,y,z) \) is expressed as

\[
\phi(x,y,z) \approx \frac{1}{2}Kz^2 - \left( \frac{1}{2}Kt_{si}^2 + Kt_{si}t_b - V_{gb}' \right) \left( \frac{z + t_g}{t_{si} + t_b + t_g} \right) + \left( \frac{t_{si} + t_b - z}{t_{si} + t_b + t_g} \right) V_{gf}' + \\
+ \frac{2R_1f_1(z)}{t_{si}a_1\Delta_1} \left[ \phi_{SD}^{(1)}(V_{gf}', V_{gb}') \cosh(\alpha_1y) \cosh(\alpha_1L/2) + \frac{1}{2}V_D \sinh(\alpha_1y) \right] \times \\
\times \left\{ 1 - \frac{\cosh(\lambda_{11}x)}{S_{11}(t_s) \cosh(\lambda_{11}W/2)} \right\} + \Omega_1(V_{gf}', V_{gb}') \frac{\cosh(\lambda_{11}x)}{S_{11}(t_s) \cosh(\lambda_{11}W/2)}
\]

(1)

Where

\[ f_1(z) = \sin(\alpha_1z) + \alpha_1t_g \cos(\alpha_1z), \]

\[ \phi_{SD}^{(1)}(V_{gf}', V_{gb}') = V_{bi} + \frac{1}{2}V_D + \frac{K}{\alpha_1^2} - \frac{1}{R_1} \left( V_{gf}' + Q_1V_{gb}' \right), \]

followed by

\[ \Omega_1(V_{gf}', V_{gb}') = V_{fb}' - V_{fB}' + \frac{K}{\alpha_1^2} + \frac{Q_1}{R_1} \left( V_{gf}' - V_{gb}' \right), \]

\[ V_{gf}' = V_{gf} - V_{fB}', \]

\[ V_{gb}' = V_{gb} - V_{fB}', \]

and

\[ V_{gs}' = V_{gf} - V_{fB}'. \]

Here \( V_{FB}'^{f,s} \) represents front, back and side gate flat-band voltages respectively. The built-in potential for n\(^*-\)p junction is \( V_{bi} = E_g/2 + \psi_b \) where \( E_g \) is energy band gap and \( \psi_b \) is the Fermi potential, \( \psi_b = (kT/q) \times \ln(N_A/n_i) \). Other parameters are \( q \)-electronic charge, \( k \)-Boltzmann constant, \( T \)-absolute temperature, \( N_A \)-doping concentration and \( n_i \) is the intrinsic concentration. The rest of the constants are defined as

\[ Q_1 = \frac{\alpha_1^2t_g^2 + 1}{\alpha_1^2t_b^2 + 1}, R_1 = 1 + Q_1, \]

\[ \Delta_1 = 1 + \alpha_1^2t_g^2 + \left( \frac{t_b + t_g}{t_{si}} \right) \left( \frac{\alpha_1^2t_b t_g + 1}{\alpha_1^2t_b^2 + 1} \right), \]

\[ S_{11}(t_s) = 1 + \lambda_{11}t_s \tanh(\lambda_{11}W/2), \]

\[ t_g = (\varepsilon_{si}/\varepsilon_{ox})t_{ox}, \]

\[ t_b = (\varepsilon_{si}/\varepsilon_{ox})t_{box}, \]

\[ t_s = (\varepsilon_{si}/\varepsilon_{ox})t_{sox}, \]
\[ \lambda_{11}^2 = \alpha_1^2 + \beta_1^2, \]

and

\[ \beta_1 = \frac{\pi}{L}, \]

\[ \alpha_1 = \frac{\pi}{2} \left( t_b + t_g \right) + \sqrt{\left( \frac{\pi}{2} \left( t_b + t_g \right) \right)^2 + 4 \left( t_b t_g + t_{si} t_b + t_{si} t_g \right)} \frac{2 \left( t_b t_g + t_{si} t_b + t_{si} t_g \right)}{2 \left( t_b t_g + t_{si} t_b + t_{si} t_g \right)}. \]

Here, \( \alpha_1^{-1} \) is the characteristic length, \( \varepsilon_0 \) is the vacuum dielectric constant and \( \varepsilon_{si} \) is the relative permittivity of silicon. On the basis of derived surface potential given in equation (1) for 3-D n-channel SOI MOSFET a sub threshold current model using the drift diffusion current equation [7] is developed. The sub threshold current, \( I_D \) can be rewritten as

\[ I_D = \left( q \mu_n \frac{t_{si}}{L} \right)^n \left( \frac{kT}{q} \right)^2 \left( 1 - e^{-\beta V_D} \right) \times \int_{-W/2}^{W/2} \int_{-L/2}^{L/2} e^{\beta \phi_s} dxdy \quad (2) \]

Where \( \mu_n \) is the carrier mobility, \( \beta = q/kT, \phi_s = \phi(x, y, z = 0) \) is the surface potential, \( L_e = L - l_S - l_D \) is the effective channel length, \( l_S \) and \( l_D \) are source-channel junction and drain-channel junction length respectively. The results of subthreshold characteristic are discussed in the next section.

III. RESULTS AND DISCUSSIONS

The subthreshold current is independent of drain voltage as it can be seen from equation (2). The variation of subthreshold current for different values of channel length and width is shown in Fig.2. As the device dimensions are decreasing the subthreshold current is increasing. In Fig.3 the plot of subthreshold current verses front gate voltage for two different values of doping concentration is presented. The subthreshold current is depending weakly on the doping concentration; the reason is that the thickness of SOI film is less as compared to the back oxide; however it is clear from Fig.3 that high doping is required to make the threshold voltage positive. The results of present model are in a good agreement with that of ATLAS simulator. It confirms the validity of 3-D subthreshold current model for SOI MOSFETs. The model can be used for deciding the important subthreshold characteristics of the device.
IV. CONCLUSION

A new three-dimensional analytical model for the subthreshold current of the fully depleted SOI MOSFET for uniform doping of channel has been developed. In our model we have depicted the doping effect on subthreshold current which can be improved by increasing the doping concentration. The model simply describes the behavior of the devices at the sub micrometer level. Also it gives the simple and compact formulae which can be implemented in circuit simulators.

REFERENCES


**Biography**

**Krishna Meel** was born in the Jhunjhunu district, Rajasthan, India on June 17, 1983. She received her Bachelor's degree in Computer Science from Jai Narayan Vyas University, Jodhpur Rajasthan in 2003 and the Masters degree in Physics from Devi Ahilya Viswa Vidyalay Indore, M.P. India in 2005. She has joined BK. Birla Institute of Engineering and Technology Pilani-Raj in 2007 as a lecturer where she is working as Assistant Professor since 2013. She is the recipient of French Embassy Scholarship (EGIDE) in 2011. She is pursuing the Ph.D. degree from the Department of Physics, University of Rajasthan, Jaipur and CSIR-Centre of Electronic and Engineering Research Institute, Pilani-Rajasthan. She is an Associate Member of the Institution of Electronics and Telecommunication Engineers (IETE), India.

**R. Gopal** was born in Hamirpur (U.P.), India in April 8, 1954. He did his M.Sc. (Physics) in 1976 from K. U, Kanpur, India and Ph.D. from Institute of Technology, Banaras Hindu University, Varanasi, India in 1986. Thereafter, he joined CSIR-Central Electronics Engineering Research Institute, Pilani, (Raj.), India, as a scientist in 1989. Presently, he is working as a Chief Scientist and Professor ACSIR in the same Institute. He has been involved *ab initio* in various R&D activities related to the development of IMPATT diode, wafer-level packaging of MEMS devices, development of MEMS gyroscopes and related research. He is also involved in modelling of SOI-MOSFETs. He has published around 21 research papers in various international journals and 20 in national and international conferences. He also has two patents to his credit.

**Deepak Bhatnagar** was born in Bareilly, India, on June 18, 1960. He received his M.Sc. and Ph.D. degrees in Physics from University of Rajasthan, Jaipur, India in 1981 and 1986 respectively. He is currently a Professor in Department of Physics, University of Rajasthan, Jaipur, India. He leads a group of 10 researchers in the field of microstrip antennas and components. He has authored or coauthored over 180 papers in international and national journals and conference proceedings. His other areas of interest are dielectric relaxation properties compounds at microwave frequencies and modeling of SOI devices. Dr. Bhatnagar is a Fellow of IETE (India) and Senior Member of IEEE.