FPGA IMPLEMENTATION OF POWER EFFICIENT ALL DIGITAL PHASE LOCKED LOOP

Sarika K R¹, Haripriya P²

¹M.Tech scholar, Dept of ECE, SreeNarayanaGurukulam College of Engineering, Kadayiruppu, Kerala, India
²Asst. Professor, Dept. of ECE, SreeNarayanaGurukulam College of Engineering, Kadayiruppu, Kerala, India

ABSTRACT

In many electronic circuits components are not receiving the clock at the exact same time. The clock generated by oscillators when reaching internal components may get distorted and require a phase locked loop to address this problem. The pure digital phase locked loop is attractive because it is less sensitive to noise and operating conditions than analog PLL. An ADPLL with an adaptive prescaler and digitally-controlled oscillator (DCO) are presented in this paper and then further modified to make the ADPLL a power efficient one.

Keywords: DCO, Phase Locked Loop, Phase Frequency Detector, Sigma Delta Modulator, Time to Digital Converter.

1. INTRODUCTION

A phase-locked loop (PLL) can be considered as a control system that generates an output signal whose phase is related to the phase of an input signal. Initially it can be visualized as an electronic circuit consisting of a variable frequency oscillator and a phase detector. The oscillator generates a periodic signal and the phase detector compares the phase of that signal with the phase of the input periodic signal and adjusts the oscillator to keep the phases matched. Bringing the output signal back toward the input signal for comparison is called a feedback loop since the output is ‘fed back’ towards the input forming a loop. Keeping the input and output phase in lock step also implies keeping the input and output frequencies the same. In addition to synchronizing signals, a phase-locked loop can track an input frequency, it can also generate a frequency that is a multiple of the input frequency. Many circuits currently face the problem of clock skew so registers, flip-flops are not receiving the clock at the exact same time. The clocks are generated by oscillators, but the clocks that reach the registers and flip-flops are distorted and require a phase locked loop to address this problem. A phase locked loop ensures that the clock frequencies seen at the clock inputs of various registers and flip-flops match the frequency generated by the oscillator.

Traditionally, a PLL is made to function as an analog building block, but integrating an analog PLL on a digital chip is difficult. Analog PLLs are also more susceptible to noise and process variations. Digital PLLs allow a faster lock time to be achieved and are attractive for clock generation on high performance microprocessors. An all digital phase locked loop was implemented by understanding the analog phase locked loop concepts to obtain the same functionality. The pure digital phase locked loop is attractive because it is less sensitive to noise and operating conditions than its analog counterpart. All digital phase-locked loop (PLL), with an adaptive prescaler and digitally-controlled oscillator (DCO) are presented. Through this project, with certain modification on digitally-controlled oscillator and the entire circuit tried to achieve a more power efficient phase locked loop with faster lock time.
2. ALL DIGITAL PHASE LOCKED LOOP

The all digital phase locked loop was designed such that it is composed of four main components. The components are analogous to the analog PLL, but the implementation consists of digital components. A digitally controlled oscillator (DCO) was utilized instead of a voltage controlled oscillator. Block diagram of the implementation is shown in Fig.1.

**Figure 1: Proposed ADPLL**

Phase Frequency Detector (PFD) detects the phase and frequency mismatch of the reference clock and divided DCO clock. The PLL is locked when the PFD detects that the phase and frequency of the two clock inputs match. The output of the PFD drives the time to digital (T2D) converter. The PFD produces up and down enable signals that are interfaced to the T2D converter. The T2D converter takes these inputs and increases or decreases the control word which is fed to the decoder. This decoder was designed by modifying the general decoder to obtain the required functionality. The decoder generates a 128 bit output which is essential for controlling the DCO. The DCO clock is divided by a specific multiplication factor, and sent back to the PFD for phase and frequency comparison. The main components and their implementation will be discussed in the following sections.

2.1 Digital phase/frequency detector

The phase frequency detector is a significant aspect of the PLL because it determines whether the reference clock and divided DCO clock are in phase and are running at the same frequency. A modified D Flip-flop was utilized because the D input doesn’t change and remains high always. The output of the modified D Flip-flops enters a two input NOR gate that resets the Flip-flops if both clocks are high. The up and down signals indicate if the DCO clock needs to be increased (up is true) or decreased (down is true). The event and direction signal are necessary to create the up and down enable signals for the T2D converter. Additional circuitry between the PFD and T2D is required for the signal conversion to take place.

2.2 Time to digital converter

The time to digital converter consists of a 6 bit down counter, 6 bit up counter, and 6 bit carry ripple adder as shown in Fig.2. The phase detector controls the up counter and down counter by up and down enable signals. The initial state of the up counter is “000000” and the down counter is “111111.” The up counter and down counter values are input into the six bit adder and the output produces the seven bit control word for the DCO. The below given figure shows the connections of the T2D converter. The six bits from the adder and the carry out bit compose the seven bit control word. The converter should be active only if there is a phase and/or frequency mismatch.
2.3 Decoder

This decoder is a specific decoder that generates the digital word that controls the DCO. The decoder was designed by modifying the general decoder to obtain the required functionality. The seven bit control word from the time to digital converter is taken as the input of this decoder and produces a 128 bit output. This 127 bit output from the decoder is given as control signal for digitally controlled oscillator. This control word determines the pulse width of the output waveform of digitally controlled oscillator.

2.4 Digitally controlled oscillator (DCO)

The controlled oscillator is a key component in PLL, which is a replacement of the conventional voltage or current controlled oscillator in the fully digital PLLs. They are more flexible and usually more robust than the conventional VCO. Furthermore, the design compromise for the frequency gain in voltage or current controlled oscillator is not necessary in DCOs because the immunity of their control input is very high. In this project digitally controlled oscillator was implemented logically. The oscillator produces output waveform having high and low pluses whose pulse width is determined by the control word from the decoder.

2.5 Frequency divider part

To achieve high-speed and low-power design, it is desirable to minimize the amount of circuitry operating at high frequency. The dual-modulus approach achieves such a structure, and has been successfully used in many high speed, low-power designs. Based on the dual-modulus topology, in this work a multi-modulus divider structure is designed, which consists of a synchronous divide-by-4/5 counter as the first stage and a program and swallow counter as the second stage as in the Fig 3.

2.5.1 Divide –by -4/5 dual modulus prescaler

The control block eliminates MC controlling the divided ratio of 4 or 5 of the synchronous counter, which is a combination logic circuitry. Depending on the logic value at MC, the first stage division ratio is 4 (MC = 0) or 5 (MC = 1). Its operation can be described based on the figure4: Divide-by-4: If signal MC is low, the active circuit consists simply of a cyclic shift register; FF3 is left out (output always high), and the input to FF1 is inverted. Divide-by-5: If the input MC is high, the NAND function formed of the outputs of FF2 and FF3 is fed into FF1, resulting in a cyclic shift register with three high periods and two low periods.
2.5.2 Program counter

The design consists of four numbers of $\div 2$ circuit and three NAND gates as in figure 5. Here four D – flip – flops are connected in cascading manner with output of one flip – flop given as input to the other flip – flop and the output of each FF are given as input to the NAND gates. And finally, the output of the third NAND gate is given as reset input to the SR – Latch. If reset is high modulus control signal M = 1. For this program counter the inputs are given from the output of 16/17 prescaler.

2.5.3 Swallow counter

The Swallow Counter is one of the three building blocks (swallow counter, main counter, and dual modulus prescaler) that constitute the programmable divider commonly used in modern frequency synthesizers. The swallow counter is used to control the dual modulus prescaler which is set to either N or (N+1). At the initial reset state, the prescaler is set to a divide ratio of (N+1), but the swallow counter will change this divide ratio to N when it finishes counting S number of cycles. The frequency divider consists of a N/N+1 prescaler followed by a program and shallow counter. The program counter generates one output pulse for every P input pulses. The Swallow Counter gets its name from the idea that it “swallows” 1 from (N+1) of the dual-modulus prescaler. The swallow counter is used to control the dual-modulus prescaler which is set to either N or (N+1).
3. MODIFIED BLOCK DIAGRAM ALL DIGITAL PHASE LOCKED LOOP

Modified circuit diagram of all digital phase locked loop include a modified digitally controlled oscillator and the frequency divider part is replaced by first order sigma delta modulator as shown in the Fig. 7.

![Modified ADPLL circuit](image)

**Figure 7:** Modified ADPLL circuit

3.1 Modified digitally controlled oscillator

In proposed DCO structure, one driving strength controlled inverter cells & two NAND/NOR gates have been used as shown in figure 8. In this design, inverter cell & two NOR/NAND gates have been utilized as compared to three delay cell and one AND gate in conventional DCO. In conventional DCO, control word is applied at the binary controlled input of all the three stages but in proposed DCO designs control word is applied only at the control input of first stage.

![Modified DCO](image)

**Figure 8:** Modified DCO

3.2 Replacement of frequency divider section by sigma delta modulator

In this project a first order sigma delta modulator is used instead of frequency divider part and sigma delta modulator just functions as a signal shaping circuit. Here output from the digitally controlled oscillator is directly given to the modulator whose output is given to the phase frequency detector. This modification in the phase locked loop circuit is done to make it more energy efficient and to achieve fast lock time.

The first step in a delta-sigma modulation is delta modulation. In delta modulation the change in the signal (its delta) is encoded, rather than the absolute value. The result is a stream of pulses, as opposed to a stream of numbers as is the case with PCM. In delta-sigma modulation, the accuracy of the modulation is improved by passing the digital output through a 1-bit DAC and adding (sigma) the resulting analog signal to the input signal, thereby reducing the error introduced by the delta-modulation.

![sigma delta modulator](image)

**Figure 9:** sigma delta modulator
4. ADPLL USED IN A FREQUENCY MULTIPLIER CIRCUIT

As an application and to check functionality of the circuit with other complex circuits, it is used with a frequency multiplier circuit. For this inbuilt frequency multiplier in the Xilinx IP core is used. The output of the phase locked loop is given to input of inbuilt frequency multiplier and checked the output.

5. RESULTS AND DISCUSSION

Simulation waveform of All digital phase locked loop is given in Fig10 and Simulation waveform of ADPLL with modified digitally controlled oscillator and sigma delta modulator is shown in figure11. Figure12 shows the output waveform of inbuilt frequency multiplier proved by the Xilinx IP core in which input of the multiplier is the output from the modified ADPLL which is given to the CLK_IN pin and the output is taken from the CLK_OUT pin.

![Figure 10: Simulation result of Modified ADPLL](image1)

![Figure 11: Simulation result of Modified ADPLL](image2)

![Figure 12: Simulation result of Frequency multiplier](image3)
6. POWER ANALYSIS

The power analysis of all digital phase locked loop Fig13 and its modified circuit Fig14 was done with the help of Xpoweranalyzer provided by Xilinx.XPowerAnalyzer.

Table 1: Summary view of ADPLL

<table>
<thead>
<tr>
<th>Device</th>
<th>OnChip Power (mW)</th>
<th>Used</th>
<th>Available</th>
<th>Utilization (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Family</td>
<td>Spartan-6</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
</tr>
<tr>
<td>Part</td>
<td>xc6le</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
</tr>
<tr>
<td>Package</td>
<td>TQFP44</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
</tr>
<tr>
<td>Tmp Grade</td>
<td>Commercial</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
</tr>
<tr>
<td>Process</td>
<td>4</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
</tr>
<tr>
<td>Speed Grade</td>
<td>0</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
</tr>
<tr>
<td>Total</td>
<td>0.052</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 2: Summary view of modified ADPLL

<table>
<thead>
<tr>
<th>Device</th>
<th>OnChip Power (mW)</th>
<th>Used</th>
<th>Available</th>
<th>Utilization (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Family</td>
<td>Spartan-6</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
</tr>
<tr>
<td>Part</td>
<td>xc6le</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
</tr>
<tr>
<td>Package</td>
<td>TQFP44</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
</tr>
<tr>
<td>Tmp Grade</td>
<td>Commercial</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
</tr>
<tr>
<td>Process</td>
<td>4</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
</tr>
<tr>
<td>Speed Grade</td>
<td>0</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
</tr>
<tr>
<td>Total</td>
<td>0.052</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

From the summary view of power analysis it is found that for implementation in the same family of device, part, package and speed grade with same environment and thermal properties the total power consumed by the all digital phase locked loop was found to be 0.053w on the other hand total power consumed by the modified all digital phase locked loop was found to be .052w Which means a power reduction of 0.001w.

7. AREA ANALYSIS

Evaluation of area is done based on the device utilization summary report. Area consumed by both circuit are analysed based on device utilization summary report. Device utilization summary of ADPLL is given in table 1 and the device utilization summary of modified ADPLL is given in table 2. And found that the area consumed by the modified all digital phase locked loop is very much lower than the earlier circuit of all digital phase locked loop.
8. CONCLUSION

In many electronic circuits the clocks that are generated by oscillators, but the clocks that reach the registers and flip-flops are distorted and require a phase locked loop to address this problem. All digital phase locked loop with adaptive prescaler and Digitally-controlled oscillator (DCO) was presented. Then it is further modified by changing the digitally controlled oscillator part and replacing the frequency divider part by a sigma delta modulator as a part of improving its power efficiency. The simulated output of both the circuit was analysed and implemented on Spartan 3e FPGA board. Then power analysis is done for both circuits and found that the modified circuit show a power reduction of 0.001w. In addition to this area consumed by the modified ADPLL circuit is much less than the earlier circuit.
REFERENCES

[1] Ii-Ting Lee, Yun-Ta Tsai, and Shen-IuanLiu, A wide-range PLL using self-healing prescaler/vco in 65-nm cmos”, IEEE Transactions on very large scale integration (VLSI) systems, vol. 21, no. 2.


