EXPLOITING DESIGN OF SYNCHRONOUS COUNTERS METHOD TO DESIGN AND IMPLEMENT MOD 6 DIRECT DOWN COUNTER

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ABSTRACT

In this paper, the design of direct mod 6 down counter is proposed by using J-K Flip Flop. The counter is provided with synchronous clock pulse. The counter is implemented by using Electronic Workbench software. The design can be achieved by the logical function minimization using Karnaugh map. Vcc and Ground are used for inputs to indicate logic 1 and 0 respectively as well as LED indicators are used to indicate the output bits. The proposed design is practical to implement any modulus of direct down counters which can count from any number to zero. This can have advantage over partial decoding method to design counters which their modulus does not belong to $2^n$ sequence because partial decoding method is only practical for up counters.

Keywords: Down Counter, Mod 6 Down Counter, Synchronous Counters.


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INTRODUCTION
Counting is a fundamental function of digital circuits [1]. It can be performed by counters which are named as sequential circuits that change their states by the clock pulses applied on their inputs. They can be used in real world applications ranging from a simple display to complex microcontroller circuits. Some of the applications are digital systems, with applications in computer systems, communication equipment, scientific instruments, and industrial control [2]. Obviously, the counters’ primary function is producing a sequence of different output patterns. Hence, they also can be named as pattern generators. These sequence of pattern scan be assigned to a number of an event’s occurrences as well as it can be used to control and select each specific part of a digital system. In this way each output state of pattern indicates the performance of each distinct part of the digital system [3]. Basically, a counter is a logic circuit that counts up to a specific number. Each count is a binary number as well as called the state of the counter. Moreover, the number of states of a counter is called modulus of the counter and can be determined through the number of bits used to design the counter. Thus, an n bit counter has $2^n$ states and called as module $2^n$ counter where n is an integer number [2].

It is clear that essential elements that associated in designing the semiconductor devices are Flip Flops [4]. There are many types of Flip Flops such as SR, D, T and JK. They can be connected together to perform the function of a counter. This means a group of Flip Flops is a counter, the number of states and the modulus of the counter can be determined through the number of Flip Flops whereas each Flip Flop holds one binary bit in the output pattern of the counter. In addition, according to the connection design of the Flip Flops together and the way the counter circuits are clocked, the Counters can be categorized in to two main categories which are asynchronous and synchronous. In asynchronous counters each Flip Flop receives clock pulse from the previous Flip Flop while in the synchronous counters all the Flip Flops are receiving their clock pulses simultaneously [5].

2. BACKGROUND

2.1 J-K FLIP-FLOP
J-K Flip-flop is like the other Flip Flops while the outputs are affected by the inputs when the Clock is high for positive edges and low for negative edges, also there are two inputs associated with this type of Flip Flop which are labeled as J and K. Furthermore, if both J and K are low and the clock pulse is applied, the output will not change as it stays as the same as the previous output state. If both J and K are high, the output will toggle from the previous output state. Finally, if J and K are different and the clock is applied the output state will follow the J input [10, 11]. The advantage of J-K Flip Flop is that it does not have any invalid state as occurred in S-R Flip Fop while both S and R are high [8]. Table 1 shows the truth table of J-K Flip Flop.
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### Table 1 J-K Flip Flop Truth table

<table>
<thead>
<tr>
<th>J</th>
<th>K</th>
<th>CLK</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>↑</td>
<td>Q_n(no change)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>↑</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>↑</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>↑</td>
<td>Q_n(toggles)</td>
</tr>
</tbody>
</table>

Moreover, the J-K Flip Flop Transition table can be seen from Table (2).

### Table 2 J-K Flip Flop Transition table

<table>
<thead>
<tr>
<th>Q_n</th>
<th>Q_n+1</th>
<th>J</th>
<th>K</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>X</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>X</td>
<td>1</td>
</tr>
</tbody>
</table>

### 2.2 COUNTER MODULUS

Counters can perform up counting to a maximum state according to the number of Flip Flops. For example, 2 bits counter has 2^2 states which can count from zero to three. This is called up counter. However, down counter produces a sequence from the maximum state to zero. For example, 3 bits counter can produce a sequence from seven to zero. In some applications, it is required that the counter should perform both up and down counting which is called up/down counter [6]. According to number of Flip Flops in the counters, the modulus of the counters is 2,4,8,16,32 and etc. This is because of that the number of states is 2^n where n is the number of Flip Flops. However, some applications might need a modulus which is not in the 2^n sequence such as modulus 4, 6, 7 and 9. In this case, there should be a mechanism to reset the counter after the maximum required state such as modulus 6 counts from 0 to 5 and should be cleared at the state of 6. This mechanism is called partial decoding [5]. In addition, this mechanism is only practical for up counters while it doesn’t work for down counters. The aim of this paper is to exploit synchronous counter design to implement a practical high performance synchronous down counter which its modulus doesn’t belong to the 2^n sequences such as modulus 6 down counter as a case study by using Electronic Workbench Software.

In this paper, Electronics Workbench (EWB) has been used to design and simulate the circuit since it is friendly as well as it provides an interface as close as to the real implementation environment [7].It provides TTL logic levels (+Vcc) used to indicate logic high for the inputs. It also provides an output circuit which is called “indicator lamp” to represent the output state of a single bit, it indicates logic high in case when it turns on, and else it indicates logic 0 [9].

### 3. DESIGNING AND TESTING THE MOD 6 DOWN COUNTER

To start with, synchronous counters need some special mathematical calculations. This can be done by drawing the counter state diagram as can be seen from Figure (1).
After that, the table of the counter’s logical function can be built as it is shown in table (3). This can be done by listing each present state of the counter with the corresponding next state [5].

<table>
<thead>
<tr>
<th>Present State (Qₙ)</th>
<th>Next State (Qₙ₊₁)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q₂ Q₁ Q₀</td>
<td>Q₂ Q₁ Q₀</td>
</tr>
<tr>
<td>1 0 1</td>
<td>1 0 0</td>
</tr>
<tr>
<td>1 0 0</td>
<td>0 1 1</td>
</tr>
<tr>
<td>0 1 1</td>
<td>0 1 0</td>
</tr>
<tr>
<td>0 1 0</td>
<td>0 0 1</td>
</tr>
<tr>
<td>0 0 1</td>
<td>0 0 0</td>
</tr>
<tr>
<td>0 0 0</td>
<td>1 0 1</td>
</tr>
</tbody>
</table>

Then, Karnaugh map can be used to calculate and determine the logic input of each J and K of each Flip Flop as shown in figure 2.
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Finally, the proposed counter can be designed by using the logic functions found through the Karnaugh Maps by using Electronic Work Bench Software as shown in figure 3.

As can be seen from the above figure the modulus 6 down counter was designed using 3 flip flops where the flip flop corresponding to Q₀ is Least Significant Bit while the one corresponding to Q₂ is Most Significant Bit. Flip Flops are clocked synchronously with negative transition of the input clock pulse (C). It is clear that the three output indicators are initially off because the counter is initially in 0 state which is 000 in binary. However, when a negative transition of the C input is applied synchronously, the counter output will change to 5 which is 101 in binary. This can be seen in figure 4.
If another clock pulse is applied to the counter. It will change its state to 4. Moreover, with each negative transition of the input clock pulse the counter decrease by 1 until it reaches 0. Then, it will repeat its sequence from 5 to 0 again. The above method can be exploited to design those down counters which there modulus do not follow $2^n$ sequences.

4. CONCLUSION

In conclusion, J-K Flip Flops were used to design the synchronous mod 6 down counter. The input of each J and K of the Flip Flops can be determined through the counter’s logical function and Karnaugh map. The proposed counter was designed and implemented by using electronic workbench software which is sufficient for designing purposes. The counter could count from 5 to 0 by applying synchronous clock pulses to the negative edges of each Flip Flop. It can be suggested that the exploited method to design the counter is practical to design any modulus of direct down counters as well as for up counters.

REFERENCES


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