DESIGN OF A UHF BAND LNA USING ACTIVE INDUCTOR WITH FFP NOISE CANCELLING TECHNIQUE

VIKAS KUMAR and R. S. GAMAD

Department of Electronics & Instrumentation Engineering,
Shri G. S. Institute of Technology and Science, Indore.

ABSTRACT

This paper reports an area-efficient LNA design using an active inductor which can be realised in various UHF band receivers. The overall low noise performance of LNA is achieved by cancelling the inductor noise through additional feed forward path. This circuit is implemented using 0.18µm CMOS technology with cadence environment and its operating range is 0.4 to 1 GHz. Design is simulated in virtuoso simulator and simulation results are measured. Noise figure is 1.6 to 3.0 dB for the UHF band and power dissipation of overall circuit is 14.03 mw at 1.8V supply.

KEYWORD: Cadence, MOS based Active Inductor, Feed forward path logic (FFP), Low Noise Amplifier (LNA), Spectre Simulator.

1. INTRODUCTION

LNA is the first signal processing block in the receiving chain of any receiver thus its noise figure and voltage gain have the most significant impact on the sensitivity level. Also linearity and power consumption need to be considered in their design. Inductor used at gate terminal of LNA with parallel resistance can be used for matching which having resonance with the amplifier input capacitance results in greater noise figure more than 3 dB, this structure is only used in narrow band application such as RF identification (RFID) [1][2]. Resistive feedback can also be used for input impedance matching with the noise cancellation path introduced in may result in reduced noise figure but it suffers from high power consumption and limited bandwidth [3] [4].
The common gate/source circuit can provide real input impedance matching but in both structure inductors is often an off-chip component because passive on chip inductors has low quality factor as well as large die area and lack of tenability. Thus need of active inductor is potentially generated. However the poor noise and linearity performance of active inductor has limited their use at LNA input in replacing passive inductors [5-9]. This design has used active inductor as input matching circuit with feed forward path to noise cancellation. The proposed LNA is fully on chip with small area and having high voltage gain as well as low noise figure and good linearity.

2. ACTIVE INDUCTOR USING MOS TECHNOLOGY

The most common topology of active inductor is shown in figure 1 using two back to back transconductances $G_{m1}$ and $G_{m2}$ (a gyrator) and a capacitor [10, 11]. The input impedance of the circuit is inductive and given as

$$Z_{in} = \frac{G_{m1}G_{m2}}{C_{p}}$$

Where, $Z_{in} = \text{Equivalent Input Impedance}$.

$G_{m1}$ (combination of transistor $M_1$ & $M_2$) & $G_{m2}$ (of transistor $M_3$) are back to back transconductance of Gyraor structure. The circuit realization of gyrator concept ($G_{m1}$and$G_{m2}$) is provided in [8][12][13] for which input impedance is inductive with high quality factor and higher resonant frequency. The inductance of the above inductor can be calculated by hybrid-$\pi$ small signal model and calculated as:
L = Inductance of Equivalent gyrator circuit. 
C is the total capacitance seen at the gate. 
g\text{m}_1 \& g\text{m}_3 \text{ are transconductance of transistor M}_1 \& M_3 \text{ respectively.} 
Here M_1 \& M_2 \text{ are assumed to be identical.}

2.1 FEED FORWARD PATH
Further for the improvement in noise performance of the above differential stage authors have added Feed forward path (FFP) as shown in figure 2. Design schematic of Active Inductor and proposed LNA are given in figure 3 and 4 respectively.

This enhances the output current by factor A_f where A_f is the gain magnitude of FFP and given as:

\[ A_f = g_{mf} \times R_f \]  \hfill (3)
Fig. 3: Schematic of Active Inductor

Fig. 4: Schematic of proposed LNA
3. SIMULATION RESULTS AND DISCUSSION

This work is carried out under the environment of cadence software. In this work authors have implemented the design with 0.18 micro meter technology than used spectre RF simulator for simulation. Simulation results are presented with applied voltage 1.8V and operating range is 0.4 to 1- GHz. Figure 5 shows the simulation response of the gain versus frequency and measured value is represented in figure with black block. Here authors have done the SP analysis to characterize the proposed design. Analysed the values of \((S_{11} & S_{22})\) were -22.7149dB and -10.024 dB respectively shown in figure 6 and 7. Noise figure in frequency range 0.4 to 1GHz has shown in figure 7. Table 1 gives the comparison of the present results with the earlier work done in same field. From this table the authors have observed that this reported work has improved the parameters as compared the earlier published work with same technology. This work will be beneficial for young researchers, designers and manufacturers for high quality design, research and manufacturing.

![Fig. 5: Gain frequency Plot](image_url)
Fig. 6: Measured $S_{11}$ of the LNA

Fig. 7: Measured $S_{22}$ of the LNA
4. CONCLUSIONS

An LNA structure with improved active inductor implementation is presented. The noise generated by the gyrator of the active inductor is reduced by the feed forward path at the input. Thus improved noise performance of the LNA makes it suitable for the on chip input impedance matching. In addition to noise cancellation the summation of signals at output would reduce the second and third order harmonics caused by nonlinearity in FFP. The measurements shows that the overall noise performance is enhanced keeping the desirable gain and the overall dc power were low. Also the proposed LNA is capable of input matching over the entire UHF band with optimization of best desired performance.
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REFERENCES