APPLICATIONS OF IMPROVED GILBERT MULTIPLIER

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ABSTRACT

With the advancement in the field of electronics at an incredible pace, the power efficient and high-speed VLSI designs are gaining more popularity and are highly in demand. The decrease in battery weight, size and increase in the lifetime are the key factors for portable equipments. Most of the reported multipliers have very poor performance and/or become non-functional in case of low-voltage, low-power environment. This paper describes various applications of analog multiplier such as frequency doubler, modulator, demodulator etc. All the simulation work has been done on Tanner EDA tool at 45nm technology.

Keywords: VLSI, Analog Multiplier, Gilbert Cell, CMOS Technology.

1. INTRODUCTION

The growing demand of data transfer via the wireless communication systems results in the fast development of various portable products [1]. The analog multipliers are basic building blocks, used in many applications like mixers and modulators in communication systems, continuous time signal processing, automatic variable gain amplifiers, adaptive filters, and neural networks [2]. The multiplier performs a linear product of continuous signals x and y yielding an output z=kxy, where k is a constant of suitable dimension [3]. The Gilbert Cell Mixer is very useful building blocks in transceiver design [4]. Gilbert-cell mixers are among the popular classes of mixers which are used extensively in wireless transceivers. Among the important features of Gilbert-cell mixers are their large bandwidth and high conversion gain (CG) [5].
2. DESCRIPTION OF THE PROPOSED CIRCUIT

Gilbert cell has two important properties. The first property is that the small-signal gain of the circuit is a function of its tail current. The second property tells that the two transistors in a differential pair provide a simple means of steering the tail current to one of the two destinations [6], [7]. Existing 12T Gilbert cell multiplier [8] has been modified by grounding the body terminal of all the nMOS transistors and connecting the body terminal of transistor \( M_{P4} \) to \( V_{DD} \) [9]. The positive and negative terminals of the output voltage \( (V_{OUT}) \) are indicating Outp and Outn respectively in the proposed multiplier circuit of Fig. 1. Here \( V_C \) is the control voltage.

For the conditions
\[
V_{DS} \geq V_{GS} - V_m \quad \text{and} \quad V_{GS} \geq V_m
\]

Equation of the drain current in the saturation region for the nMOS is given by
\[
I_D = \frac{k_n}{2} (V_{GS} - V_m)^2
\]

All the transistors in Fig. 1 operate in the saturation region. Input signals are applied in the complementary form i.e.
\[
V_1 = -V_2 \quad \text{and} \quad V_{C1} = -V_{C2}
\]

The input signal being varied and \( 4V_1^2 \) is taken to approximately zero. So the output current [9]
\[
I_{OUT} = \frac{2\sqrt{2}R_D V_C k_n}{R_{OUT}}
\]
\[
I_{OUT} \propto V_1 V_C \quad \text{(1)}
\]

Where \( k_1 = \frac{2\sqrt{2}R_D k_n}{R_{OUT}} \)

Equation (1) indicates that the output current \( (I_{OUT}) \) is proportional to the product of input voltages which is the property of the voltage multiplier so it is a voltage multiplier.
3. SIMULATION RESULTS

In order to verify the circuit operation and characteristics, several experimental simulations have been carried out at the 45nm technology using Tanner EDA tool. The transient response of the proposed multiplier is shown in Fig. 2. Here input signals are sinusoidal with 10mv peak amplitude, frequency of $V_1$ and $V_C$ are $500kHz$ and $0.1GHz$ respectively and the supply voltage is ±0.8v. The aspect ratio of all transistors is taken 1. The proposed multiplier had power consumption and power-delay product less than the existing 12T Gilbert cell based multiplier almost 2 times and 4 times respectively [9].
4. APPLICATIONS OF PROPOSED MULTIPLIER

4.1 Frequency Doubler

When a sinusoidal voltage \( A \sin \omega t \) is applied to the both inputs of the proposed multiplier, output produced is double frequency of the input signal.

\[
V_o = A^2 \sin^2 \omega t
\]

\[
V_o = \frac{A^2}{2} (1 - \cos 2\omega t)
\]

Thus the output signal contains the DC component and cosine component of frequency \( 2\omega \), which twice of the input frequency. For example if the sinusoidal voltage of 50mv amplitude and frequency of 500kHz is given to the inputs then the output voltage is proportional to ,as shown in Fig. 3. Thus proposed multiplier can operate as frequency doubler.

4.2 Modulator

The growing demand of data transfer via the wireless communication systems results in the fast development of various portable products [10]. The purpose of a communication system is to deliver a message signal from an information source in recognizable form to a user destination, with the source and the user being physically separated from each other [11]. Modulation is the systematic alteration of one waveform, called the carrier, according to the characteristics of another waveform, the modulating signal or message [12]. A circuit, stage or piece of hardware that modulates is called a modulator.

When two sinusoidal voltages of different frequencies (500 kHz and 0.1GHz) are applied to the inputs of proposed multiplier presented in Fig. 1, the output results in a modulated sine wave as shown in Fig. 4 (a).
Fig. 4 (b) represents the triangular modulation of sine wave when one input is a sinusoidal voltage and the other is a triangular voltage of lower frequency, the output is triangular modulation of sinusoidal voltage. Thus the proposed multiplier circuit can also behave as modulator.

![Output waveform of modulator for sinusoidal input](image)

**Fig. 4(a)** Output waveform of modulator for sinusoidal input

![Output waveform of modulator for triangular input](image)

**Fig. 4(b)** Output waveform of modulator for triangular input

4.3 Demodulator

To reconstruct the transmitted signal, modulated signal must pass through a reversal process known as demodulation. A circuit, stage or piece of hardware that demodulates is called a demodulator. Proposed multiplier presented in Fig.1 can also act as demodulator after connecting capacitors at the output shown in Fig. 5.
Fig. 5 Demodulator using proposed multiplier

Transient response of the proposed multiplier as demodulator is shown in Fig. 6. In this circuit two capacitor c1 and c2, each of 0.1pf, have been used. Here input signals are sinusoidal with 50mv peak amplitude, frequency of $V_1$ and $V_C$ are 500kHz and 0.1GHz respectively and the supply voltage is ±0.8v. Where $V_1 = -V_2$ & $V_{C1} = -V_{C2}$.

Fig. 6 Output waveform of demodulator

5. CONCLUSION

Applications of the proposed multiplier have been simulated at the 45nm technology using Tanner EDA tool. Simulation results demonstrate that the proposed multiplier can act as frequency doublers when both inputs have the same frequency. It can also be used as modulator when one input has a higher frequency than other and demodulator.
REFERENCES


