MINIMIZING TEST POWER IN VLSI ARCHITECTURE USING BIST BASED LOW-TRANSITION TEST PATTERN GENERATION TECHNIQUE

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ABSTRACT

The Integrated circuit (IC) contains Built-In Self-Test (BIST) and circuit under test (CUT), to test the correct functionality of any integrated circuit, test patterns are generated from Built In Self Test and then same generated test patterns are applied to the Circuit-under-Test (CUT), minimizing hardware overhead is a major concern of BIST implementation. In pseudo-random BIST design, the test vectors are generated with the help of Linear Feedback Shift Registers (LFSR) and which is called as conventional LFSR. The main drawback of these conventional LFSRs is, it generates normally more number of random natured test vectors for testing the CUT in which many are repeated patterns and application of which unnecessarily increase the test power without contributing much to the fault coverage. Apart from this, as the bulkiness of the CUT increases, the test vector generating engine is even becomes large in terms of number of sequential or test vector generating element. So that it could generate as many numbers of vectors which can fits the number of I/O pins of CUT logic or part of CUT logic. Thus, the increase in size of test circuit also requires the considerable die size on IC.

This paper presents a new approach, called Linear feedback shift register -Bit complement test pattern generation technique (LFSR-BCTPG). In LFSR-BCTPG technique, the output bits are complemented due to which unrepeated test vectors are increased also by which better fault coverage with reduction in the bulkiness of the test circuit can be achieved. Hence, in this approach, the proposed test circuit can be half in size, compared to other conventional test circuits to test a particular CUT. The final results of proposed approach have been compared with other methods and found that, this method is better in terms of dynamic power dissipation when applying the test vectors generated by the proposed method to four different ISCAS'89 benchmark circuits.

Keywords: Linear feedback shift register- Bit complement Test Pattern Generation (LFSR- BCTPG), Bulkiness, test power and Linear feedback shift register (LFSR)
1. INTRODUCTION

Moore’s law states that the number of transistors integrated in a chip has doubled every 18 months ever since the integrated circuit was invented. As these trends continue, numerous new challenges turn out to be important in the testing of very-large-scale-integrated (VLSI) circuits. With the advance of semiconductor industrialized technology, the requirements of VLSI circuits have led to many challenges during manufacturing test. This is because of the large and complex chips which require a huge amount of test data and dissipate a substantial amount of power during testing, resulting in considerable increases in the test cost.

It is known fact that power dissipation in the circuit during the test mode is considerable compared to that in the normal mode [1]. This can be accepted to the correlation existing between consecutive test vectors applied during the normal mode of operation of the circuit. However, this is not the case in the test mode. There is no considerable correlation between consecutive vectors in the test mode. This automatically means that the primary switching activities will be more in the test mode compared to that in the normal mode and that the power dissipation will be higher in the test mode. Thus, more the transitions between the test vectors more will be the power dissipated. Hence, low power testing is the need of the hour.

This issue can be overcome by the use of Built-In-Self-Test (BIST) design. A BIST circuitry is contained as a part of the target system that aids in the verification of the internal functionality of the particular circuit it is assigned. BIST is a method of allowing test logic to be incorporated as a part of the chip itself. The BIST architecture is widely accepted because of its very many advantages like the reduction in test application time, reduction in the cost of generation of test vectors, to allow at-speed testing, to provide an alternative to the expensive Automatic Testing Equipment (ATE) and the reduction in the volume of test data. Also, the overhead area occupied by the BIST in the circuit can be considered negligible in comparison to the size of the target system [2]. The BIST makes the target system independent of any external automatic equipment for testing [1].

Hence, this proposed method aims to analyze and discuss a circuit that generates test patterns that help reduce the average and peak power dissipation in BIST architecture during testing mode. Also, efforts are made to bring about appropriate modifications to the logical and structural implementation, of the circuit under consideration, in order to reduce the power dissipation even further.

2. TEST PATTERN GENERATION

![Conventional Linear feedback shift register (LFSR)](image)

Figure 1: Conventional Linear feedback shift register (LFSR)

Test patterns are basically a set of inputs (1’s and 0’s) in BIST, which are generated by the Linear feedback shift register (LFSR) [3] of the BIST, will determine if the circuit is working as per requirement or if it is faulty when these test patterns applied on a circuit.
In the BIST, the LFSR generates the test patterns. The LFSR can either have a serial or a parallel input and provide serial or parallel output. In this case, the LFSR is that kind of shift register, wherein, the bits moves serially from the input through the registers for every clock pulse [3]. The LFSR can be made to generate pseudorandom patterns with the help of an exclusive-OR gate as shown in the above fig 1.

The vectors in the test mode may consume a higher average or peak power than that in the normal mode. The decreased correlation between the pseudorandom patterns (the patterns generated will repeat after a cycle is completed) generated by the LFSR is attributed as the reason for the additional dissipated power in test mode. This in turn ends in an increase in the switching activities of the circuit, thereby, leading to increased power dissipation [1].

2.1 Need for low power testing

The System-On-Chips platform imposes a challenge in the design and testing methodology. Testing gains the primary significance in terms of issues and expenditure, thereby, demanding a wide range of possible novelties. The area of concentration, here, is power dissipation [1]. In general, the power consumed during the test mode is more than that in the normal mode of operation. This additional power dissipated may pose a threat to the circuitry and can also lead to a breakdown of the chip. This in turns will raise the costs, increase the difficulty in verifying the performance of the circuit and thereby reduce the final code [1]. Having learnt the above, the necessity of decreasing the power dissipated in a circuit during the test mode is a major milestone for further advancements in VLSI design.

A number of reasons can be quoted for the increased power consumption in the circuit during the test mode [2]. Decreased correlation between the test vectors can be sited as the first reason. Normally, a considerable correlation exists between the inputs during the operational mode, but may not be the same in the test mode. This decreased correlation in the input during the test mode increases the switching activities, thereby increasing the power dissipation [1]. Secondly, the use of parallel testing process by test engineers in order to reduce the test application time can result in increased power dissipation. The third reason can be attributed to the DFT circuit that is inbuilt in the design for the test mode, which is normally idle during the operational mode, however, is extensively active in the test mode [2].

3. MODIFIED LOW POWER TEST PATTERN GENERATOR

3.1 LFSR - Bit complement test pattern generation technique (LFSR-BCTPG)

![Figure 2: proposed LFSR-BCTPG](image-url)
In Conventional LFSR, many of the test patterns will usually be repeated out of generated random nature test pattern set and application of which on any benchmark circuits (CUT) results in more internal switching activities causing more unnecessary dynamic power dissipations without even contributing much to the fault coverage.

Generally, the test vector generating engine will have as many sequential elements as the CUT has the input pins. Thus, the output of the test vector generating circuit can be interfaced with the CUT. In this method, the test vector generating engine requires to be very large in case the CUT has higher gate counts or higher input pads.

Hence, for testing a particular CUT, the normal test vector generating circuit has been reduced by inverting it’s half of the output vectors as shown in fig2. This way, the actual length of the test vector generating engine can be reduced to half of it’s actual size. Thus, in this method Conventional LFSR is reduced to half of its actual size from which test patterns are generated and at the same time generated test patterns are complemented by adding additional inverters to each output to get the same number of outputs which achieved by conventional LFSR and the design is called LFSR - Bit complement test pattern generation technique (LFSR-BCTPG). The most of the test patterns generated from LFSR-BCTPG are non repeated compare to conventional LFSR there by Dynamic power dissipation is reduced. Also by LFSR-BCTPG technique, the bulkiness of BIST is greatly minimized thereby chip area of the testing circuit is reduced as shown in the fig2.

Here, en1 and en2 enable signals are used. In which, signal en1 is connected to the first eight flip-flops and en2 is connected to the last eight flip-flops. If en = ‘1’, then the respective half of the flip flops to which the en signal is connected are active and the values pertaining to those flip flops are shifted to the right. However, if en = ‘0’, the half of the flip flops to which the signal is connected are in the idle mode and hence, do not shift their input values to the right and retains the previous values at their outputs.

**Table 1**

<table>
<thead>
<tr>
<th>Clk</th>
<th>Pattern</th>
<th>en1</th>
<th>en2</th>
<th>LP-BCTPG</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Pi</td>
<td>1</td>
<td>0</td>
<td>1010 1011 1010 1011</td>
</tr>
<tr>
<td>2</td>
<td>Pk1</td>
<td>0</td>
<td>0</td>
<td>1010 1111 1010 1111</td>
</tr>
<tr>
<td>3</td>
<td>Pk2</td>
<td>0</td>
<td>1</td>
<td>1010 0101 1010 0101</td>
</tr>
<tr>
<td>4</td>
<td>Pk3</td>
<td>0</td>
<td>0</td>
<td>1111 0101 1111 0101</td>
</tr>
<tr>
<td>5</td>
<td>Pi+1</td>
<td>1</td>
<td>0</td>
<td>0101 0101 0101 0101</td>
</tr>
</tbody>
</table>

Referring to the Fig2. LFSR-BCTPG circuit, the ‘first part flops’ (before the dummy block) are ff1, ff2, ff3, ff4, ff5, ff6, ff7 and ff8. Also, the ‘second part flops’ (after the dummy block) are ff9, ff10, ff11, ff12, ff13, ff14, ff15, ff16.

**Step 1:** en1=1, en2 = 0
As en1=1, the first part flops will be in active mode. As en2=0, the second part flops will be in idle mode.

**Step 2:** en1=0, en2 = 0
As en1=0 and en2 =0, both part of the flip flop will be in idle mode.

**Step 3:** en1=0, en2 = 1, sel1=1, sel=1
As en1=0, the first part flops will be in idle mode. As en2=1, the second part flops will be in active mode.

**Step 4:** en1=0, en2 =0, sel1=0, sel2 =1
As en1=0 and en2 =0, both part of the flip flop will be in idle mode.

**Step 5:** The procedure as in step 1 is repeated here and vector Pi+1 is generated.
The above method continues from step 1 through step 5 for as many clock cycles as is required.

The complete circuit is controlled by a finite state machine (FSM), as is shown in the below circuit that acts as the gear stick in the generation of the test patterns. The FSM serves as the control unit for the generation of the test patterns by continuing through steps 1 to 4.

As we can be observe, the intermediary vectors $P_{k1}$, $P_{k2}$ and $P_{k3}$ are generated between two consecutive random vectors $P_1$ and $P_2$. It is seen that the number of transitions between $P_1$ and $P_2$ are 7. However, the transitions between $P_1$ & $P_{k1} = 1$, $P_{k1}$ & $P_{k2} = 2$, $P_{k2}$ and $P_{k3} = 2$ and that between $P_{k3}$ and $P_2 = 2$. This shows that the correlation between two successive test vectors being significantly reduced after the introduction of the three intermediary vectors which reduces power dissipation within CUT by minimizing the switching activities.

4. EXPERIMENTAL RESULTS

The test patterns generated by LFSR and LFSR-BCTPG are shown in TABLE 2 are used for verifying the ISCA85 benchmark circuit C17, S27, and S298. Simulation and synthesis are done in Xilinx 14.1 and switching power is carried out of table 3 are done using Spy Glass. Programming of the design is done in Verilog and simulation of the design is carried out using MODEL SIM 6.2.

<table>
<thead>
<tr>
<th>Circuit Under Test (CUT)</th>
<th>32-bit LFSR</th>
<th>Proposed LFSR-BCTPG</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>C17</td>
<td>S27</td>
</tr>
<tr>
<td>Leakage Power</td>
<td>2.19nW</td>
<td>3.84nW</td>
</tr>
<tr>
<td>Internal Power</td>
<td>195.86nW</td>
<td>258.16nW</td>
</tr>
<tr>
<td>Switching Power</td>
<td>104.19nW</td>
<td>417.12nW</td>
</tr>
<tr>
<td>Total Power</td>
<td>302.25nW</td>
<td>679.128nW</td>
</tr>
</tbody>
</table>

TABLE 2 shows the Switching power dissipation of the 32bit Conventional LFSR. The test patterns which are generated from this 32bit Conventional LFSR are applied to the three different 32bit benchmark circuits C17, S27 and S298.

5. COMPRESSION RESULT

From TABLE 2 experimental results shows that Switch power dissipation of the benchmarks circuit C17 for proposed LFSR-BCTPG indicate up to 35.65% reduction in switching power compare to conventional LFSR, similarly S27 reduction in 22.67% and S298 reduction of 14.98%. It is concluded that linear feedback shift register Bit complement test pattern generation (LFSR-BCTPG) is very much useful for power optimization in BIST.
6. FAULT COVERAGE

The test patterns generated by LFSR, LP-BCTPG and LP-BITPG are shown in TABLE 5, TABLE 6 and TABLE 7 is used for verifying the ISCA85 benchmark circuit C17, S27 and S298. Simulation and synthesis are done in Xilinx 14.1 and power analysis is done using Spy Glass. Programming of the design is done in Verilog and simulation of the design is carried out using MODEL SIM 6.2.

<table>
<thead>
<tr>
<th>Circuit Under Test (CUT)</th>
<th>Expected Patterns for 16-bit</th>
<th>No. of Non repeated test pattern</th>
<th>No. of repeated test pattern</th>
<th>No. of gates</th>
<th>Fault Coverage (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>32-bit LFSR</td>
<td>C17</td>
<td>65536</td>
<td>65058</td>
<td>192</td>
<td>99.23</td>
</tr>
<tr>
<td></td>
<td>S27</td>
<td>65536</td>
<td>65050</td>
<td>192</td>
<td>99.25</td>
</tr>
<tr>
<td></td>
<td>S298</td>
<td>65536</td>
<td>65536</td>
<td>192</td>
<td>99.24</td>
</tr>
<tr>
<td>Proposed LFSR-BCTPG</td>
<td>C17</td>
<td>65536</td>
<td>60790</td>
<td>96</td>
<td>92.37</td>
</tr>
<tr>
<td></td>
<td>S27</td>
<td>65536</td>
<td>60538</td>
<td>96</td>
<td>92.37</td>
</tr>
<tr>
<td></td>
<td>S298</td>
<td>65536</td>
<td>60790</td>
<td>96</td>
<td>92.37</td>
</tr>
</tbody>
</table>

From TABLE 3 experimental results of Benchmark circuit C17, S27 and S298 show that fault coverage is decreased to 92.37%, 92.37% and 92.37% respectively in proposed LFSR-BCTPG compare to conventional LFSR but the number of gates required to design testing circuit is decreased to 50% hence bulkiness of the chip is decreased almost half of the conventional LFSR.
7. CONCLUSIONS

This paper presents a new Linear feedback shift register - Bit complement test pattern generator technique (LFSR-BCTPG). Power consumption of LFSR-BCTPG is reduced due to the bit Complement technique and also the bulkiness of the circuit is reduced to half of the conventional LFSR. LFSR-BCTPG provides greater randomness than Conventional LFSR and also which have the potential to generate all possible test patterns to detect all possible faults. The switching activity in
the CUT power consumption is reduced by increasing the correlation between patterns and also within each pattern.

8. REFERENCES


AUTHORS DETAILS

Mr. Praveen J. Completed his B.E degree in Electrical and Electronics from Kuvempu university in the year 1999, M.Tech in VLSI design and Embedded system in the year 2004 and currently pursuing his Ph.D Degree in Electronics from Mysore University, Karnataka from 2010. He is presently working as an Associate Professor in the Department of Electronics and communication, Alva’s Institute of Engineering & Technology, Moodbidri, South Canara, Karnataka, India. His areas of interest are VLSI Design and Testing. He has published two papers in the International Journals and Conferences in his field of expertise. He has delivered invited lectures and Organized a few in-house workshops and certificate programs.

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