DSPIC BASED DIGITIZED FEEDBACK LOOP FOR DC-DC CONVERTER

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ABSTRACT

This paper describes an efficient digitized feedback way-out for buck converter operating at high frequency. The designed power system uses digital control to allow the inclusion of more functionality, control schemes and flexibility in design for quick modifications. The buck converter works at 400khz switching frequency with classical PID control monitors start-up behavior and robustness to disturbances of system. The results of the switching converter system has been analyzed based on comparison of simulation of state model in matlab/simulink and actual results.

Keywords: DSPIC, state space equation, PID control

1. INTRODUCTION

![Diagram of Digitized Feedback Loop for Switching Converter]

**Figure 1:** Digitized feedback loop for switching converter
Modern DC power supplies are becoming more efficient, more flexible, less expensive and smaller. Their enhancement has been achieved by incorporating digital signal controllers into Switch Mode Power Supply (SMPS) based designs. Buck converters are used when the desired output voltage is lower than the input voltage. Usually, the non-linear behavior of switch creates control problem consists of defining the desired nominal operating condition, and then regulating the circuit so that it stays close to the nominal reference voltage. Use of PID controller improves the steady state performance and transient response. It is possible to design stable, efficient and ruggedized SMPS which has faster transient response for dynamically switching loads. [1]

Synchronous buck converters with voltage-mode control and voltage-mode error amplifier have received great attention in low voltage DC/DC converter applications because they can offer high efficiency; provide more precise output voltage and also meet the size requirement constraints.

2. DESIGN OF SYNCHRONOUS BUCK CONVERTER

![Synchronous buck converter](image)

Figure 2: Synchronous buck converter

The designed synchronous buck converter system accepts 9V, 2A and provides 2V,4W output. The digital PWM signals provided to the switching MOSFETs are operated around 400kHz frequency. The part of system’s output is feed to the dsPIC based computational unit compromising of ADC where the digital voltage output obtained is compared with the reference voltage to produce an error signal. The error signal is further processed to modify the pulse width of DPWM to stabilise the output.

3. STEADY STATE ANALYSIS OF BUCK CONVERTER

Power electronics converters are system having periodic time variation, because of their switching operation. In general, state space averaging method models the converter as time independent system, defined by a unique set of differential equations, capable of representing circuit waveforms. Therefore, it proves be a convenient approach for designing controllers to be applied to switched converters [3]. The state diagram The source code further stabilises the DC output to around ± 2% of the desired output by incooperating the PID compensation. The digital computation unit used is using dsPIC33FJ16GS502 instead of using DSP processor for obtaining economical but efficient solution over analog feedback system, which suffers variation due to environmental factors, ageing [3][7]. Buck of converter is simulated using matlab/simulink.
The differential equation for the system for the state variables obtained from figure 3 are Applying KVL and KCL to the loop:

\[ L \frac{di_L(t)}{dt} = V_{in}(t) - R_{ON}i_L(t) - R_Li_L(t) - V_{out}(t) \]  

(1)

\[ i_C(t) = i_L(t) - i_R(t) \]  

(2)

\[ C \frac{dv_C(t)}{dt} = i_L(t) - \frac{V_{out}(t)}{R} \]  

(3)

State equations obtained are:

\[
\begin{bmatrix}
L & 0 \\
0 & C
\end{bmatrix}
\begin{bmatrix}
\frac{di_L(t)}{dt} \\
\frac{dv_C(t)}{dt}
\end{bmatrix}
= \begin{bmatrix}
-R_{ON} + R_L + (R||R_C) \\
\frac{R}{R + R_C}
\end{bmatrix} \begin{bmatrix}
i_L(t) \\
v_C(t)
\end{bmatrix} - \frac{R}{R + R_C} \begin{bmatrix}
i_L(t) \\
v_C(t)
\end{bmatrix} + \begin{bmatrix} 1 \\ 0 \end{bmatrix} V_{in}(t)
\]
(4)

\[
\begin{bmatrix}
V_{OUT}(t) \\
i_{IN}(t)
\end{bmatrix}
= \begin{bmatrix}
\frac{R}{R + R_C} \\
0
\end{bmatrix} \begin{bmatrix}
\frac{R}{R + R_C} \\
0
\end{bmatrix} \begin{bmatrix}
i_L(t) \\
v_C(t)
\end{bmatrix} + \begin{bmatrix} 1 \\ 0 \end{bmatrix} V_{in}(t)
\]
(5)
Applying KCL and KVL for figure 4

\[ \frac{dL}{dt} \left[ \frac{\partial L}{\partial t} \right] = -[R_{ON}i(t) + R_Li(t) + V_{out}(t)] \]  

\[ V_{out}(t) - V_C(t) - i_C(t)R_C = 0 \]  

The state equations obtained are

\[ \begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix} \begin{bmatrix} \frac{dL}{dt} \\ \frac{dV_C}{dt} \end{bmatrix} = \begin{bmatrix} -R \left[ R_{ON} + R_L + (R||R_C) \right] \frac{R}{R + R_C} \frac{1}{R + R_C} \end{bmatrix} \begin{bmatrix} i(t) \\ V(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} V_{in}(t) \]  

\[ \begin{bmatrix} V_{OUT} \\ i_{IN} \end{bmatrix} = \begin{bmatrix} [(R||R_C)] \frac{R}{R + R_C} \frac{R}{R + R_C} \\ 0 \end{bmatrix} \begin{bmatrix} i(t) \\ V(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} V_{in}(t) \]  

The state equations are used to obtained the model to be simulated in matlab/simulink. The buck converter model simulated results are close to actual results.

4. MINIMUM RESOLUTION OF A/D CONVERTER, DIGITAL PWM:

To satisfy specifications for the voltage regulation of output and to limit the oscillation produced due to fast switching, resolution of the A/D converter has to enable error lower than the allowed variation of the output voltage \( \Delta V_0 \).

\[ n_{a/d} = int[log_2 \frac{V_{maxa/d}}{V_{ref}} \frac{V_0}{\Delta V_0}] \]  

Equation (1) gives the minimum number of bits for the A/D converter to meet the design specifications in terms of the output voltage regulation. For example, if 2\% variation.[2]

Digital pulse width modulator (DPWM) produces a discrete set of duty ratio values. This means that in steady state only a discrete set of output voltage values can be obtained.

\[ n_{PWM} \geq int[n_{a/d} + log_2 \left( \frac{V_{ref}}{V_{maxa/d}} \right)] \]  

From equation (2) reveals that the minimum resolution of the DPWM depends on steady-state operating conditions in the circuit and the A/D resolution [2].

The dsPIC33FJ16GS502 digital computation unit used in this paper has 10 bit ADC and the frequency resolution of PWM is 1.04ns. These dsPIC ICs have features like DSP processors. Hence a comparatively efficient but low cost and lesser complex switching system is achieved using dsPIC IC[1]. The source code incorporates the calculation of PID coefficient to assure closed loop stability of the system. This controller has one pole at the origin and two zeros. The equation PID controller, shown in Equation (3)

\[ G_C(s) = K_p + \frac{K_i}{s} + K_d(s) \]  

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5. EXPERIMENTAL RESULTS

A) Simulated output voltage = 2.1v

B) Practical Output voltage: 2.080v

C) Simulated PWM: 400 KHz

D) Practical pwm_h = 391.1khz

E) Practical pwm_l = 391.1khz
Table 1: overall result

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Simulink Output</th>
<th>Practical output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output voltage</td>
<td>2.10v</td>
<td>2.080v</td>
</tr>
<tr>
<td>PWM frequency</td>
<td>400Khz</td>
<td>391.1KHz</td>
</tr>
<tr>
<td>PWM duty cycle</td>
<td>60%</td>
<td>75%</td>
</tr>
</tbody>
</table>

Table 2: Practical parameters obtained

<table>
<thead>
<tr>
<th>parameter</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$</td>
<td>9V</td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>2V</td>
</tr>
<tr>
<td>Input Power</td>
<td>18W</td>
</tr>
<tr>
<td>Output Power</td>
<td>4W</td>
</tr>
<tr>
<td>PWM-H</td>
<td>10.60V, 391.1 KHZ</td>
</tr>
<tr>
<td>PWM-L</td>
<td>10.60V, 391.1 KHZ</td>
</tr>
</tbody>
</table>

6. CONCLUSION

This paper explores digital controlled power supply systems with objective of the achieving improvements in converter control schemes, system performance over conventional analog control approaches and cost effectiveness lesser complex system over most popular and efficient DSP processor. Digital controllers, provides a favorable position to provide basic feedback control as well as power management functions with lower cost and great flexibility. The design and implementation 400 Khz high frequency buck converter system using dsPIC controller is described.

7. REFERENCES

8. Muhammad Saad Rahman “Buck Converter Design Issues” Master thesis performed in division of Electronic Devices