MULTI-INPUT QUASI-FLOATING GATE MOSFETS WITH ANALOG INVERTER USED IN CIRCUITS

S.K BisoI, G. Devi

ABSTRACT

The multiple-input floating gate transistors were used to simplify the design of multiple valued logic. The Quasi-floating gate node have a well defined DC operating point. The multi-input quasi-floating gate is used for low voltage applications because its effective threshold voltage will be controlled to a low value.

Keywords: Quasi-floating gate, multi-input quasi-floating gate, analog inverter.

1. INTRODUCTION

The floating gate MOS transistor is generated by forming an additional conductive layer between control terminal and channel DS isolated from environment called floating gate [10]. Multiple-input floating gate MOS transistor is a floating gate transistor with multiple control gate. The input control gates are capacitively coupled to the floating gate [8,9].

Floating gate is contacting with the channel through the capacity of oxide layer and with source, drain and bulk. The values of these capacities depend on the area of input gate, floating gate and channel as well as on thickness of oxide layer [5,6]. The whole MIFGMOS transistor made on semiconductor. The main goals are to release the traditional semi-floating designs from recharge mode and to implement in continuous mode. Quasi floating gate can compute multiple valued signals and obtain higher frequencies [1,2,3,4]. The analog inverter is a key element in multiple valued logic. The transfer characteristic of the analog inverter is determined by capacitor division factor

\[ K_I = \frac{C_i}{C_{Total}} \quad \text{and} \quad V_{out} = V_{dd} - V_{in} \]

where \( V_{in} \) and \( V_{out} \) are the voltages on the input and output terminal and \( V_{dd} \) is supply voltage.
II. MULTI INPUT QUASI FLOATING GATE

Since Quasi floating gate node have a well defined DC operating point and this technique is used for low voltage applications, so that multi input QFG can compute multiple valued signals and obtain higher frequencies. To operate the function of CMOS transistors at the output of inverter, the gate terminals of inverter must be biased through the DC supply voltage and that will be provided through the coupling capacitors \( C_{gb} \) and \( C_{gb'} \) and hence, Quasi floating MOS gates are proposed to provide a DC shift to the combined AC signal.

The quasi floating MOS gates are operating at +5v or -5v depending on n-type and p-type MOS gates. This supply voltage or some portion of supply voltage may pass through the channel from source to drain or drain to source depending on n-type and p-type MOS gate. The leakage resistors and the parallel capacitors are operate in such a manner that the combined AC signals can pass through the capacitors and DC signals can block through the capacitors in the Quasi floating MOS gates so that the DC shifting on positive side or negative side of the combined AC signal can be done depending on types of MOS gates.

The shifting of AC signals are required to only provide the debiasing to the gate terminals of CMOS inverter and that is not directly provided at gate terminal, but through the coupling capacitors which can store the DC voltage due to high impedance and pass the AC signal without shift due to low impedance.

The coupling capacitors are DC block capacitors i.e. in DC signals, \( f=0\text{Hz} \).

\[
X_c = \frac{1}{\omega C} = \frac{1}{2\pi fC} = \infty \Omega \quad \text{(Open circuit path)}
\]

and in AC signal, \( f = \text{very high} = \infty \text{Hz} \)

\[
X_c = \frac{1}{\omega C} = \frac{1}{2\pi fC} = 0\Omega \quad \text{(Short circuit path)}
\]

that is the coupling capacitors are short circuit paths.

At input side terminals the capacitors are provided to pass the high frequency signals only and if any DC signal or low frequency signals accommodate with the original signals that can be nullify and pure form of high frequency signals can easily pass through the capacitors.

The combinations of signals are generated at the node point which then passes through the quasi floating MOS gates and then MOS inverter operation obtain.
\[ C_i = C_{1}, C_{2}, C_{3}, C_{ds} (\text{with } R_{\text{leak}} \text{ n-mos }), C_{gb} (\text{at the inverter}) \]
\[ C_{4}, C_{5}, C_{6}, C'_{ds} (\text{with } R_{\text{leak}} \text{ p-mos }), C'_{gb} (\text{at the inverter}) \]
\[ C_{sd} (\text{at the output}) \]

\[ V_{i} = V_{1}, V_{2}, V_{3} \]
\[ V_{qfg} \]
\[ V_{4}, V_{5}, V_{6} \]
\[ R_L \rightarrow \text{Load Resistance at Output} \]

III. SIMULATION AND MODEL

\[ V_{QFG} = V_{in} \frac{s \cdot R_{\text{leak}} \cdot C_{\text{Total}}}{1 + s \cdot R_{\text{leak}} \cdot C_{\text{Total}}} \]
where \( C_{\text{Total}} = \sum_{i=1}^{n} C_i + C_{GS} + C_{GD} + C_{GB} + C'_{GD} \)

and \( V_{in} = \frac{1}{C_{\text{Total}}} \left( \sum_{i=1}^{n} C_i \cdot V_i + C_{GS} \cdot V_S + C_{GD} \cdot V_D + C_{GB} \cdot V_B \right) \)

\[ V_{QFG1} = \frac{1}{C'_{\text{Total}}} \left( \sum_{i=1}^{n} C'_i \cdot V'_i + C_{GS} \cdot V_S + C_{GD} \cdot V_D + C_{GB} \cdot V_B \right) \]
\[ \left( \frac{s \cdot R_{\text{leak}} \cdot C_{\text{Total}}}{1 + s \cdot R_{\text{leak}} \cdot C_{\text{Total}}} \right) \]

\[ V_{QFG2} = \frac{1}{C'_{\text{Total}}} \left( \sum_{i=1}^{n} C'_i \cdot V'_i + C_{GS} \cdot V_S + C_{GD} \cdot V_D + C_{GB} \cdot V_B \right) \]
\[ \left( \frac{s \cdot R'_{\text{leak}} \cdot C'_{\text{Total}}}{1 + s \cdot R'_{\text{leak}} \cdot C'_{\text{Total}}} \right) \]

where, \( C_{\text{Total}} = \sum_{i=1}^{n} C'_i + C_{GS} + C_{GD} + C_{GB} + C''_{GD} \)

and \( V_{in} = \frac{1}{C'_{\text{Total}}} \left( \sum_{i=1}^{n} C'_i \cdot V'_i + C_{GS} \cdot V_S + C_{GD} \cdot V_D + C_{GB} \cdot V_B \right) \)

It is in Ohmic mode or triod region that is \( V_{GS} > V_{th} \) and \( V_{DS} < \left( V_{QFG} - V_{th} \right) \)

\[ I_{DS} = \mu_n C_{ox} O/L \left( V_{QFG} - V_{th} \right) \left( V_{DS} - \frac{V_{DS}^2}{2} \right) \]

![Fig. 1](image1.png)
![Fig. 2](image2.png)
Composed base band signals with capacitors, "Vin2".
IV. CONCLUSION

In this paper we have presented a new multi-input Quasi floating gate with analog inverter used in circuit. It offers better frequency response with larger band width and large leakage resistance needs less chip area as compared to its multiple input floating gate technique.

REFERENCE

AUTHOR’S INFORMATION

Sunil Bisoi is studying for his Ph.D in the field of Neural networks in Utkal University. His research activities and interest include VLSI realization of Neural networks and analogue integrated circuits and systems. Bisoi received the Engineering degree from Utkal University. He is an Associate Professor of ENTC department in Orissa Engineering College, Odisha.

Dr. Gayatri Devi heads the PG department of computer science and engineering at Ajay Binay Institute of Technology of Odisha. Her current field of interest in MOS integrated circuits and systems and application of Neural Networks.

Devi received PG degree in Math from Utkal University and engineering degree (B.Tech in ETC and M.Tech in CSC) from Raisthan Deemed University and Ph.d & D.Sc degree from Utkal University of Odisha. She is a member of IEEE, Odisha Information technology of society and Odisha Mathematical Society.