AN OPTIMIZED HIGH SPEED DUAL MODE CMOS DIFFERENTIAL AMPLIFIER FOR ANALOG VLSI APPLICATIONS

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ABSTRACT

The differential amplifiers play a very important role in the analog circuit design because of their excellent performance as input amplifiers and the straightforward application with the possibility of feedback to the input. The classical differential amplifier faces the disadvantage of the nonlinearity of the transfer characteristic, especially for large values of the differential input voltage amplitude. The differential amplifier circuit characterized in terms of self-bias capability, common-mode rejection, voltage gain, and the gain-bandwidth product. This highly improved linear multifunctional circuit can be used for VLSI applications, with an immediate advantage of increased modularity and controllability and the reduced design costs associated represent an immediate consequence of the multiple functions realized by the proposed structure: amplifying, multiplying or simulating positive and negative resistances. In this paper, we report a new model of an optimized high speed dual mode CMOS differential amplifier. The proper selection of device parameters has been playing an important role in the design of differential amplifier. This model is simulated in pSPICE simulator and optimized device parameters for level 3 parameters using 0.2μm CMOS technology.

Keywords: Differential amplifier, dynamic range, settling time, analog design, frequency compensation, high-speed design, stability, folded cascode, single stage, Differential mode, Common Mode, CMRR, Transconductance, current Sink.

I. INTRODUCTION

The differential amplifier is one of the most versatile circuits used in analog circuit design. These are widely used in the electronics industry and are generally preferred over their single-ended counterparts because of their better common-mode noise rejection, reduced
harmonic distortion, and increased output voltage swing \([1, 2, 3]\). The differential amplifiers are used to amplify analog as well as digital signals, and can be used in various implementable applications so as to provide an output from the amplifier in desired response to the differential inputs. It is also very compatible with integrated circuit technology and serves as the input stage to most of operational amplifier \([3, 4, 5, 6, 7]\). These circuits can be readily adapted to behave as an operational amplifier, a comparator, an instrumentation amplifier, etc. The differential amplifier is often a building block or sub-circuit used within high-quality integrated circuit amplifiers, linear and nonlinear signal processing circuits, and even certain logic gates and digital interfacing circuits in various VLSI applications. In recent years, there has been an increasing demand for a system-on-chip configuration (SOC) and reduction of power consumption, in response to which the CMOS has been widely used \([4, 8, 9, 10, 11]\).

CMOS based differential amplifiers are used for various VLSI applications because a number of advantages can be derived from these types of amplifiers, as compared to single-ended amplifiers. These amplifiers are used where linear amplification with minimum distortion is desired. The common mode feedback is accomplished by the use of a common mode feedback circuit that monitors the two differential amplifier output lines and provides a feedback signal that adjusts the amplifier's bias current, thereby rejecting the unwanted common mode signals on the amplifier's output. The sensitivity is an important specification target for differential amplifier design \([12]\). A very important trend in VLSI designs, especially for submicron technologies is the continuous reducing of the layout area i.e. the parasitic bipolar transistors and especially classical resistors having a surface consumption proportional to the value of the resistance represent the largest area consumers. Thus, it is not efficient to obtain resistances greater than 10 K\(\Omega\) using the classical approach. The new method for reducing the occupied area for large values of the equivalent resistance is to implement a circuit named active resistor using exclusively CMOS transistors for simulating a linear current-voltage characteristic. An important class of these circuits, referring to the active resistors with controllable negative equivalent resistance, covers a specific area of VLSI designs, findings very large domains of applications such as the canceling of an operational amplifier load or the design of integrators with improved performances \([13, 15]\).

![Fig1: Basic Two Stage Topology of Differential Amplifier](image)

In choosing the topology of the amplifier, following parameters are kept in the design consideration i.e.

- High dynamic range of the amplifier so as to ensure the minimum noise level at the output.
- Fast settling time of the amplifier ensures large flow of currents to charge the capacitor so as to minimize the slew rate limitations.
The maximum total output noise that the circuit could tolerate for a given output swing which has direct effect on determining the size of the compensation capacitor and feedback capacitor to give the desired dynamic range i.e. [16, 17, 18]

\[
DR = 10 \log \frac{P_{\text{peak}}}{P_{\text{noise}}} = 10 \log \left[ \frac{1}{8} \left( \frac{V_{\text{max}}}{V_n} \right)^2 \right] \geq 90 \text{db} \quad (1) \]

\[
SR = \frac{I_1}{C_c} \quad (2)
\]

Similarly, the settling time for the CMOS devices of the amplifier which is a combination of “linear” & “Slewing” settling times and is given as, with

\[
t_s = t_{\text{slew}} + t_{\text{lin}} \leq 5 \text{ns} \quad (3)
\]

In order to minimize power consumption, while meeting the settling requirement, it is desired to use \( C_c \) as small as possible limited by the dynamic range requirement. Secondly, if we select the frequency, about 1/3 and \( V_o \), in a step, about 2.5 V, for fixed value of \( C_c \), the total settling time decreases as \( V_{\text{dsat}} \) decreases [19, 20].

II. BASIC DIFFERENTIAL AMPLIFIERS CONFIGURATIONS

The below shown figures give us the basic configurations of the differential amplifiers with different mode of connections [21, 22, 23, 24, 25].

![Differential Amplifier Configurations](image)

Now let us assume that \( v_{\text{IN1}} >> v_{\text{IN2}} \), with \( M_1 \) and \( M_2 \) has same threshold voltage i.e. the transistor \( M_1 \) derives much faster than \( M_2 \) i.e. [26]

\[
i_{d1} > i_{d2} \quad (4) \quad i_{d1} + i_{d2} = I \quad (5)
\]

Again, we also assume that both of the transistors are in saturation then [27, 28],

\[
i_{d1} = K_N (v_{\text{GS1}} - V_t)^2 \quad (6) \quad i_{d2} = K_N (v_{\text{GS2}} - V_t)^2 \quad (7)
\]

where

\[
K_N = \frac{\mu_n C_{ox}}{2} \left( \frac{W}{L} \right) \quad (8)
\]
Thus, it is observed that the transistors in the fig 2(b) are perfectly matched due to which it always operate in saturation region. Based on this concept, the large signal analysis of the circuit can be given as [27, 29]:

\[ V_{1D} = V_{GS1} - V_{GS2} = \left( \frac{2I_{D1}}{\beta} \right)^{\frac{1}{2}} - \left( \frac{2I_{D2}}{\beta} \right)^{\frac{1}{2}} \]  \hspace{1cm} (9) \hspace{1cm} I_{DS1} = i_{DS1} = i_{DS2}  \hspace{1cm} (10)

thus, the relation of the drain currents can be given as

\[ i_{DS1} = \frac{I_{ss}}{2} + \frac{I_{ss}}{2} \left( \frac{\beta V_{1D}^{2}}{I_{ss}} - \frac{\beta V_{1D}^{4}}{4I_{ss}^{2}} \right) \]  \hspace{1cm} (11)

\[ i_{DS2} = \frac{I_{ss}}{2} - \frac{I_{ss}}{2} \left( \frac{\beta V_{1D}^{2}}{I_{ss}} - \frac{\beta V_{1D}^{4}}{4I_{ss}^{2}} \right) \]  \hspace{1cm} (12)

Also the desired relation for the most dominant parameter of the differential amplifier i.e. transconductance can be given as [30, 34]:

\[ g_{m} = \left( \frac{K_{1}I_{ss}W_{1}}{4L_{1}} \right)^{\frac{1}{2}} \]  \hspace{1cm} (13)

From this above relation (13), it is observed that the transconductance is directly proportional to \( I_{ss} \) current i.e. as \( I_{ss} \) increases the value of the transconductance \( (g_{m}) \) also increases.

III. PROPOSED CMOS BASED DIFFERENTIAL AMPLIFIER

The proposed differential amplifier is shown in Fig. 3(a) and 3(b) with the two modes of the operation i.e. the differential mode of operation and the common mode configuration respectively. These circuits provide a better differential gain and very small common mode gain. Thus, the CMRR of the proposed differential amplifier is extremely high as compared to the basic one. The transistor M3 and M7 forms the input stage of differential amplifier and M2 and M1 are for the output stage. Transistor M4 and M6 are used for current sink. The differential input is applied between the gate terminals of M3 & M7, the output can be taken across the drain of M1 and M2. The proposed structure is simulated for W/L=1 in order to obtain the proper matching. The simulation in differential mode is carried out by taking step signal as input to gate terminal of M7 and the gate of M3 is ground. In order to analysis the common mode gate of M7 and M3 is shorted and then step input is applied for simulation. For this same, this simulation of the circuit has been carried out at level 3 parameters using 0.2\( \mu \)m CMOS technology.
The mathematical relation for the transconductance of the differential amplifier is given as [35]:

$$g_{mD} = \frac{\Delta I}{\Delta V_{ID}} = \frac{2\Delta I}{\Delta V_{ID}} = \frac{\Delta I}{V_{g1}} = g_{m1} \quad (14)$$

$$A_{VDO} = \frac{V_2}{V_1} = \frac{V_o}{V_{id}} = \frac{g_{m1}}{g_{ds2} + g_{ds4}} = \frac{g_{m2}}{g_{ds2} + g_{ds4}} \quad (15)$$

And the dc voltage gain of the differential amplifier is given as [36]:

IV. SIMULATION RESULTS

The transient response analysis for the differential mode and the common mode of the CMOS based differential amplifier is shown in figures 4(a) and 5(a). From this analysis result, one can observe that the voltage at input terminal ($V_2$) is amplified at the output terminal ($V (10, 5)$) in differential mode. And in case of the common mode, it is almost zero which shows that the amplifier has very high CMRR. The figures 4(b) and 5(b) shows the ac and the noise performance analysis of the differential mode and the common mode respectively. The ac analysis plots the input and output noise contributed to the circuit from various possible sources. This result shows that the circuit works properly up to the 5 MHz frequency. It means that beyond this frequency the performance of the circuit becomes poor i.e. deteriorates. The figures 4(c) and 5(c) show the voltage transfer characteristic of the amplifier in the differential mode and the common mode configurations. Here it is observed that the differential mode curve is linear for input voltage range between -3.14 volts to +3.14 volts. Thus, the proposed circuit is most suitable for low voltage VLSI applications, where as in the common mode configuration, the graph is non linear and noisy but it can be used for the signal in the range of nano volts. This shows that in common mode configuration, the output voltage is very-very small which also confers that the CMRR is very high. So this circuit can be used in the design of low voltage high CMRR operational .amplifier, Fileters, VCOs, etc. The fig 5(d) shows the dc analysis of the proposed circuit of the differential amplifier in common mode configuration that depicts that the amplifier is operating in very much correlation to the input signal. It simply replicated the input with the maximum possible linearity and minimum and well optimized delay the circuit is taking in providing the output.
V. CONCLUSIONS

In this paper a high performance CMOS differential amplifier circuit has been proposed. This circuit best suited for low voltage and high common mode rejection ratio (CMRR) applications. The input voltage can be applied between -3.14 volts to +3.14 volts and its performance is better up to 5 MHz. The circuit can be used in design of low voltage and CMRR operational amplifiers, Operational transconductance amplifiers, Voltage controlled oscillators (VCO).

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REFERENCES

[31]. Ramakant A. Gayakward, Op-Amps and Linear Integrated Circuits : Pearson Education